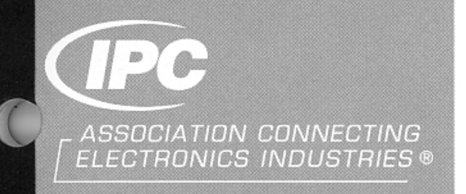



# IPC-7351

## Generic Requirements for Surface Mount Design and Land Pattern Standard

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A standard developed by IPC

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# Generic Requirements for Surface Mount Design and Land Pattern Standard

## 1 SCOPE

This document provides information on land pattern geometries used for the surface attachment of electronic components. The intent of the information presented herein is to provide the appropriate size, shape and tolerance of surface mount land patterns to insure sufficient area for the appropriate solder fillet to meet the requirements of IPC/EIA J-STD-001, and also to allow for inspection, testing, and rework of those solder joints.

**1.1 Purpose** Although, in many instances, the land pattern geometries can be different based on the type of soldering used to attach the electronic part, wherever possible, land patterns are defined with consideration to the attachment process being used. Designers can use the information contained herein to establish standard configurations not only for manual designs but also for computer-aided design systems. Whether parts are mounted on one or both sides of the board, subjected to wave, reflow, or other type of soldering, the land pattern and part dimensions should be optimized to insure proper solder joint and inspection criteria.

Land patterns are dimensionally defined and are a part of the printed board circuitry geometry, as they are subject to the producibility levels and tolerances associated with plating, etching, assembly or other conditions. The producibility aspects also pertain to the use of solder mask and the registration required between the solder mask and the conductor patterns.

**Note 1:** The dimensions used for component descriptions have been extracted from standards developed by industrial and/or standards bodies. Designers should refer to these standards for additional or specific component package dimensions.

**Note 2:** For a comprehensive description of the given printed board and for achieving the best possible solder joints to the devices assembled, the whole set of design elements includes, beside the land pattern definition:

- Soldermask.
- Solder paste stencil.
- Clearance between adjacent components.
- Clearance between bottom of component and PCB surface, if relevant.
- Keepout areas, if relevant.
- Suitable rules for adhesive applications.

The whole of design elements is commonly defined as "mounting conditions." This standard defines land patterns and includes recommendations for clearances between adjacent components and for other design elements.

**Note 3:** Elements of the mounting conditions, particularly the courtyard, given in this standard are related to the reflow soldering process. Adjustments for wave or other soldering processes, if applicable, have to be carried out by the user. This may also be relevant when solder alloys other than eutectic tin lead solders are used.

**Note 4:** This standard assumes that the land pattern follows the principle that, even under worst case conditions, the overlap of the component termination and the corresponding soldering land will be complete.

**Note 5:** Heat dissipation aspects have not been taken into account in this standard. Greater mass may require slower process speed to allow heat transfer.

**Note 6:** Heavier components (greater weight per land) require larger lands; thus, adding additional land pattern surface will increase surface area of molten solder to enhance capabilities of extra weight. In some cases the lands shown in the standard may not be large enough; in these cases, considering additional measures may be necessary.

**Note 7:** The land form may be rectangular with straight or rounded corners. In the latter case the area of the smallest circumscribed rectangle shall be equal to that of one with straight corners.

**1.2 Documentation Hierarchy** This standard identifies the generic physical design principles involved in the creation of land patterns for surface mount components, and is supplemented by a shareware IPC-7351 Land Pattern viewer that provides, through the use of a graphical user interface, the individual component dimensions and corresponding land pattern recommendations based upon families of components. The IPC-7351 Land Pattern Viewer is provided on CD-ROM as part of the IPC-7351. Updates to land pattern dimensions, including patterns for new component families, can be found on the IPC website (www.ipc.org) under "PCB Tools and Calculators." See Appendix C for more information on the IPC-7351 Land Pattern Viewer.

**1.2.1 Component and Land Pattern Family Structure** The IPC-7351 provides the following number designation within the IPC-7350 series for each major family of surface mount components to indicate similarities in solder joint engineering goals:

IPC-7352 – Discrete Components
IPC-7353 – Gullwing Leaded Components, Two Sides
IPC-7354 – J-Leaded Components, Two Sides
IPC-7355 – Gullwing Leaded Components, Four Sides
IPC-7356 – J-Leaded Components, Four Sides
IPC-7357 – Post (DIP) Leads, Two Sides
IPC-7358 – Area Array Components (BGA, FBGA, CGA)
IPC-7359 – No Lead Components (QFN, SON, LCC)

**1.3 Performance Classification** Three general end-product classes have been established to reflect progressive increases in sophistication, functional performance requirements and testing/inspection frequency. It should be recognized that there may be an overlap of equipment between classes.

The end product user has the responsibility for determining the "Use Category" or "Class" to which the product belongs. The contract between user and supplier shall specify the "Class" required and indicate any exceptions or additional requirements to the parameters, where appropriate.

*Class 1 General Electronic Products* – Includes consumer products, some computer and computer peripherals, and hardware suitable for applications where the major requirement is function of the completed assembly.

*Class 2 Dedicated Service Electronic* – Products Includes communications equipment, sophisticated business machines, and instruments where high performance and extended life is required, and for which uninterrupted service is desired but not mandatory. Typically the end-use environment would not cause failures.

*Class 3 High Reliability Electronic Products* – Includes all equipment where continued performance or performance-on-demand is mandatory. Equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support systems and other critical systems.

The IPC-7351 land patterns have the capability of accommodating all three performance classifications.

**1.3.1 Producibility Levels** When appropriate this standard will provide three design producibility levels of features, tolerances, measurements, assembly, testing of completion or verification of the manufacturing process that reflect progressive increases in sophistication of tooling, materials or processing and, therefore progressive increases in fabrication cost. These levels are:

*Level A General Design Producibility – Preferred*
*Level B Moderate Design Producibility – Standard*
*Level C High Design Producibility – Reduced*

The producibility levels are not to be interpreted as a design requirement, but a method of communicating the degree of difficulty of a feature between design and fabrication/assembly facilities. The use of one level for a specific feature does not mean that other features must be of the same level. Selection should always be based on the minimum need, while recognizing that the precision, performance, conductive pattern density, equipment, assembly and testing requirements determine the design producibility level. The numbers listed within the tables of IPC-7351 are to be used as a guide in determining what the level of producibility will be for any feature. The specific requirement for any feature that must be controlled on the end item shall be specified on the master drawing of the printed board or the printed board assembly drawing.

Classification of producibility levels should not be confused with density levels of land pattern geometries described in 1.4.

**1.4 Land Pattern Determination** This standard discusses two methods of providing information on land patterns.

1. Exact details based on industry component specifications, board manufacturing and component placement accuracy capabilities. These land patterns are restricted to a specific component, and have an identifying IPC-7351 land pattern name.
2. Equations can be used to alter the given information to achieve a more robust solder connection, when used in particular situations where the equipment for placement or attachment are more or less precise than the assumptions made when determining the land pattern details (see 3.1.2).

Three land pattern geometry variations are supplied for each of the device families; maximum land protrusion (Density Level A), median land protrusion (Density Level B) and minimum land protrusion (Density Level C). Before adapting the minimum land pattern variations the user should consider product qualification testing based on the conditions shown in Table 3-15.

***Density Level A: Maximum (Most) Land Protrusion*** – For low-density product applications, the 'maximum' land pattern condition has been developed to accommodate wave or flow solder of leadless chip devices and leaded gull-wing devices. The geometry furnished for these devices, as well as inward and "J"-formed lead contact device families, may provide a wider process window for reflow solder processes as well.

***Density Level B: Median (Nominal) Land Protrusion*** – Products with a moderate level of component density may

consider adapting the 'median' land pattern geometry. The median land patterns furnished for all device families will provide a robust solder attachment condition for reflow solder processes and should provide a condition suitable for wave or reflow soldering of leadless chip and leaded gull-wing type devices.

***Density Level C: Minimum (Least) Land Protrusion*** – High component density typical of portable and hand-held product applications may consider the 'minimum' land pattern geometry variation. Selection of the minimum land pattern geometry may not be suitable for all product use categories. The use of classes of performance (1, 2, and 3) is combined with that of component density levels (A, B, and C) in explaining the condition of an electronic assembly. As an example, combining the description as Levels 1A or 3B or 2C, would indicate the different combinations of performance and component density to aid in understanding the environment and the manufacturing requirements of a particular assembly.

**Note:** It is the responsibility of the user to verify the SMT land patterns used for achieving an undisturbed mounting process, including testing and an ensured reliability for the product stress conditions in use. In addition the size and shape of the proposed land pattern may vary according to the solder resist aperture, the size of the land pattern extension (dog bone), the via within the extension, or if the via is in the land pattern itself.

### 1.5 Terms and Definitions

Terms and definitions used herein are in accordance with IPC-T-50 except as otherwise specified. **Note:** Any definition denoted with an asterisk (*) is a reprint of the term defined in IPC-T-50.

****Assembly*** – A number of parts, subassemblies or combinations thereof joined together. (**Note:** This term can be used in conjunction with other terms listed herein, e.g., "Printed Board Assembly.")

***Assembly, Double-Sided*** – Packaging and interconnecting structure with components mounted on both the primary and secondary sides.

***Assembly, Multilayer Printed Circuit (wiring)*** – Multilayer printed circuit or printed wiring board on which separately manufactured components and parts have been added.

***Assembly, Packaging and Interconnecting (P&IA)*** – Generic term for an assembly that has electronic components mounted on either one or both sides of a packaging and interconnecting structure.

***Assembly, Printed Board*** – An assembly of several printed circuit assemblies or printed wiring assemblies, or both.

***Assembly, Printed Circuit (wiring)*** – A printed circuit or printed wiring board on which separately manufactured components and parts have been added.

***Assembly, Single-Sided*** – Packaging and interconnecting structure with components mounted only on the primary side.

****Base Material*** – The insulating material upon which a conductive pattern may be formed. (The base material may be rigid or flexible, or both. It may be a dielectric or insulated metal sheet.)

****Basic Dimension*** – A numerical value used to describe the theoretical exact location of a feature or hole. (It is the basis from which permissible variations are established by tolerance on other dimensions in notes or by feature control symbols.)

****Blind Via*** – A via extending only to one surface of a printed board.

****Buried Via*** – A via that does not extend to the surface of a printed board.

****Castellation*** – A recessed metalized feature on the edge of a leadless chip carrier that is used to interconnect conducting surface or planes within or on the chip carrier.

****Chip Carrier*** – A low-profile, usually square, surface-mount component semiconductor package whose die cavity or die mounting area is a large fraction of the package size and whose external connections are usually on all four sides of the package. (It may be leaded or leadless.)

****Chip-On-Board (COB)*** – A printed board assembly technology that places unpackaged semiconductor dice and interconnects them by wire bonding or similar attachment techniques. Silicon area density is usually less than that of the printed board.

****Coefficient of Thermal Expansion (CTE)*** – The linear dimensional change of a material per unit change in temperature. (See also "Thermal Expansion Mismatch.")

****Component*** – An individual part or combination of parts that, when together, perform a design function(s). (See also "Discrete Component.")

****Component Mounting Site*** – The location on a Package Interconnect (P&I) structure that consists of a land pattern and conductor fan-out to additional lands for testing or vias that are associated with the mounting of a single component.

****Conductive Pattern*** – The configuration or design of the conductive material on a base material. (This includes conductors, lands, vias, heatsinks and passive components when these are an integral part of the printed board manufacturing process.)

****Conductor*** – A single conductive path in a conductive pattern.

***Constraining Core** – A supporting plane that is internal to a packaging and interconnecting structure.

***Courtyard*** – The smallest rectangular area that provides a minimum electrical and mechanical clearance (courtyard excess) around the combined component body and land pattern boundaries.

***Courtyard Excess*** – The area between the rectangle circumscribing the land pattern and the component, and the outer boundary of the courtyard. The courtyard excess may be different in the x- and y-direction.

***Courtyard Manufacturing Zone*** – The area that provides a minimum electrical and mechanical clearance (courtyard excess) around the combined component body and land pattern boundries.

***Dual-Inline Package (DIP)** – A basically-rectangular component package that has a row of leads extending from each of the longer sides of its body that are formed at right angles to a plane that is parallel to the base of its body.

***Fine-Pitch Technology (FPT)** – A surface-mount assembly technology with component terminations on less than 0.625 mm [0.025 in] centers.

***Fiducial (Mark)** – A printed board artwork feature(s) that is created in the same process as the conductive pattern and that provides a common measurable point for component mounting with respect to a land pattern or land patterns.

***Flat Pack** – A rectangular component package that has a row of leads extending from each of the longer sides of its body that are parallel to the base of its body.

***Footprint** – See "Land Pattern."

***Grid** – An orthogonal network of two sets of parallel equidistant lines that is used for locating points on a printed board.

***Integrated Circuit (IC)** – A combination of inseparable associated circuit elements that are formed in place and interconnected on or within a single base material to perform a particular electrical function.

***Jumper wire** – A discrete electrical connection that is part of the original design and is used to bridge portions of the basic conductive pattern formed on a printed board.

***Land** – A portion of a conductive pattern usually used for the connection and/or attachment of components.

***Land Pattern** – A combination of lands that is used for the mounting, interconnection and testing of a particular component.

***Leadless Chip Carrier** – A chip carrier whose external connections consist of metallized terminations that are an integral part of the component body. (See also "Leaded Chip Carrier.")

***Leaded Chip Carrier*** – A chip carrier whose external connections consist of leads that are around and down the side of the package. (See also "Leadless Chip Carrier.")

***Master Drawing** – A control document that shows the dimensional limits or grid locations that are applicable to any and all parts of a product to be fabricated, including the arrangement of conductors and nonconductive patterns or elements; the size, type, and location of holes; and all other necessary information.

***Mixed Component-Mounting Technology*** – A component mounting technology that uses both through-hole and surface-mounting technologies on the same packaging and interconnecting structure.

***Module** – A separable unit in a packaging scheme.

***Nominal Dimension*** – A dimension that is between the maximum and minimum size of a feature. (The tolerance on a nominal dimension gives the limits of variation of a feature size.)

***Packaging and Interconnecting Structure (P&IS)** – The general term for a completely processed combination of base materials, supporting planes or constraining cores, and interconnection wiring that are used for the purpose of mounting and interconnecting components.

***Plated-Through Hole (PTH)** – A hole with plating on its walls that makes an electrical connection between conductive patterns on internal layers, external layer, or both, of a printed board.

***Primary Side** – The side of a packaging and interconnecting structure that is so defined on the master drawing. (It is usually the side that contains the most complex or the most number of components.)

***Printed Board (PB)** – The general term for completely processed printed circuit and printed wiring configurations. (This includes single-sided, double-sided and multilayer boards with rigid, flexible, and rigid-flex base materials.)

***Printed Wiring** – A conductive pattern that provides point-to-point connections but not printed components in a predetermined arrangement on a common base. (See also "Printed Circuit.")

***Registration** – The degree of conformity of the position of a pattern (or portion thereof), a hole, or other feature to its intended position on a product.

***Secondary Side** – That side of a packaging and interconnecting structure that is opposite the primary side. (It is the same as the "solder side" on through-hole mounting technology.)

***Single-Inline Package (SIP)** – A component package with one straight row of pins or wire leads.

***Static Charge*** – An electrical charge that has accumulated or built up on the surface of a material

***Static Electricity Control*** – A technique where materials and systems are employed to eliminate/discharge static electricity build-up by providing continuous discharge paths

****Supported Hole*** – A hole in a printed board that has its inside surfaces plated or otherwise reinforced.

****Supporting Plane*** – A planar structure that is a part of a packaging and interconnecting structure in order to provide mechanical support, thermo-mechanical constraint, thermal conduction and/or electrical characteristics. (It may be either internal or external to the packaging and interconnecting structure.) (See also "Constraining Core.")

****Surface Mount Technology (SMT)*** – The electrical connection of components to the surface of a conductive pattern that does not utilize component holes.

****Tented Via (Type I Via)*** – A via with a mask material (typically dry film) applied bridging over the via wherein no additional materials are in the hole. It may be applied to one side or both.

****Thermal Mismatch*** – The absolute difference between the thermal expansion of two components or materials. (See also "Coefficient of Thermal Expansion (CTE).")

****Through Connection*** – The electrical connection to connect conductor patterns on the front side through to the back side of a printed board. (See also "Interfacial Connection.")

****Through-Hole Technology (THT)*** – The electrical connection of components to a conductive pattern by the use of component holes.

****Tooling Feature*** – A physical feature that is used exclusively to position a printed board or panel during a fabrication, assembly or testing process. (See also "Locating Edge," "Locating Edge Marker," "Locating Notch," "Locating Slot," and "Tooling Hole.")

****Via*** – A plated-through hole that is used as an interlayer connection, but in which there is no intention to insert a component lead or other reinforcing material. (See also "Blind Via" and "Buried Via.")

## 2 APPLICABLE DOCUMENTS

### 2.1 IPC[1]

**IPC-A-48** Surface Mount Land Pattern Artwork (Mantech)

**IPC-A-49** Surface Mount Land Pattern Artwork (IPC-SM-782)

**IPC-T-50** Terms and Definitions for Interconnecting and Packaging Electronic Circuits

**IPC-A-610** Acceptability of Printed Board Assemblies

**IPC-SM-785** Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

**IPC-S-816** SMT Process Guideline and Checklist

**IPC-1902** Grid System for Printed Circuits

**IPC-2221** Generic Standard on Printed Board Design

**IPC-2226** Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

**IPC-2581** Generic Requirements for Printed Board Assembly Products Manufacturing Description Data and Transfer Methodology

**IPC-6012** Qualification and Performance Standard for Rigid Printed Boards

**IPC-7095** Design and Assembly Process Implementation for BGAs

**IPC-7525** Stencil Design Guidelines

**IPC-7530** Guidelines for Temperature Profiling for Mass Soldering Processes

**IPC-7711/21** Rework and Repair Guide

**IPC-9701** Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments

### 2.2 Electronic Industries Association[2]

**EIA-481** Tape and Reel Specification

### 2.3 Joint Industry Standards (IPC)[3]

**J-STD-001** Requirements for Soldered Electrical and Electronic Assemblies

**J-STD-002** Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

**J-STD-003** Solderability Tests for Printed Boards

**J-STD-033** Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

1. www.ipc.org
2. www.eia.org
3. www.ipc.org

## 2.4 International Electrotechnical Commission[4]

**IEC-61188** Printed Boards and Printed Board Assemblies - Design and Use

## 2.5 Joint Electron Device Engineering Council (JEDEC)[5]

**Publication 95** JEDEC Registered and Standard Outlines for Solid State Products

# 3 DESIGN REQUIREMENTS

**3.1 Dimensioning Systems** This section describes a set of dimensional criteria for components, land patterns, positional accuracy of the component placement capability and the opportunity to create a certain size solder joint commensurate with reliability or product performance analysis.

Profile tolerances are used in the dimensioning system to define the size range between maximum and minimum component/lead dimensions without ambiguity. The profile tolerance is intended to control both size and position of the land. Figure 3-1 shows the profile tolerancing method.

The use of the profile dimensioning system requires an understanding of the concepts. The use of a set of requirements are adopted and invoke the following rules, unless otherwise modified.

a. All dimensions are basic (nominal).
b. Limits of size control form as well as size.
c. Perfect form is required at maximum dimensions.
d. Datum references and position tolerances apply at maximum dimensions, and are dependent on feature size.
e. Position dimensions originate from maximum dimensions.
f. Tolerances and their datum references other than size and position apply regardless of feature size (RFS).

The dimensioning concepts used for this system of analysis consider the assembly/attachment requirements as their major goal. Specification (data) sheets for components or dimensions for land patterns on boards may use different dimensioning concepts, however, the goal is to combine all concepts into a single system. Users are encouraged to establish the appropriate relationship between their dimensioning system(s) and the profile dimensioning system and analysis concepts described herein to allow for ease of tailoring these concepts for robust process performance. As an example, if the tolerance used for positioning is larger than the machine tolerance used in production, a single dimensional change could modify the land pattern.

**3.1.1 Component Tolerancing** The component manufacturers and industry standards organizations are responsible for the dimensioning and tolerancing of electronic components (see 3.1.5.2). The basic dimensions and tolerance limits published in the specifications have been converted to a functional equivalent using the profile tolerancing method with all components shown with their basic dimensions as limit dimensions (maximum or minimum size). Profile tolerances are unilateral, and are described to reflect the best condition for solder joint formation.

The concept for component dimension evaluations is based on evaluating the surfaces of the component termination and component lead or contact that are involved in the

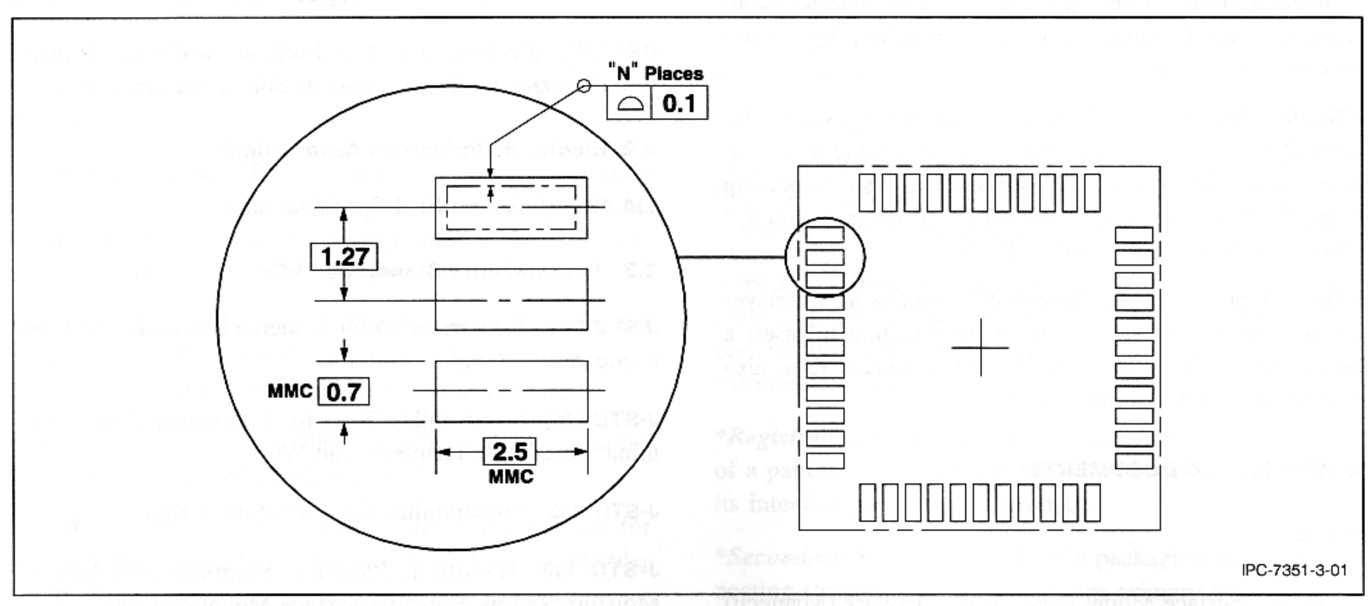



**Figure 3-1 Profile Tolerancing Method**

4. www.iec.ch
5. www.jedec.org

formation of the acceptable solder joint. Component manufacturers usually provide dimensions for their parts with a nominal size and then put a tolerance on that nominal dimension. In order to facilitate the dimensioning system, these dimensions and their associated tolerances are converted to minimum and maximum size.

As an example, capacitor C3216 has a manufactured nominal dimension for its length of 3.2 mm. The tolerance described by the manufacturer is ± 0.2 mm. Thus, the minimum dimension of "L" is 3.0 mm with a unilateral tolerance of 0.4 mm, resulting in its maximum dimension being 3.4 mm.

Figure 3-2 shows the characteristics for the 3216 capacitor. Item A in Figure 3-2 shows the component manufacturer's dimensions for the length of the capacitor. Item B in Figure 3-2 shows the component length at its minimum size in the converted dimensions of the new system using profile tolerancing. Item C in Figure 3-2 shows the land pattern at its maximum size. These conditions provide for an optimum toe fillet. For optimum heel fillet, the component basic dimensions are at the maximum and the land pattern is at its minimum.

Similar concepts are applied to leaded surface mount parts. The critical dimensional characteristics identified are those that relate to the formation of the toe and heel solder fillet. For components with gull-wing leads, the basic dimensions apply across the outer extremities of the part for toe land projection; and within the inside of the formed radius of opposing leads for heel solder fillet formation.

The outer dimensions of leaded or even leadless chip carriers are usually easy to determine since these are readily available from the component manufacturer or standards organization. The inner (heel-to-heel) dimensions are not provided in industry standards or manufacturers' specifications and are more difficult to determine, not only because of the form of the lead, termination, or castellation but also because the inner dimensions must be derived by subtracting the sum of the dimensions of the leads (with all their inherent tolerances) from the overall dimensions of the part.

Item A in Figure 3-3 shows the concept for the manufacturer's dimensions and tolerances for a gull-wing SOIC. Item B in Figure 3-3 shows the converted dimensions to be considered in the overall mounting system requirements.

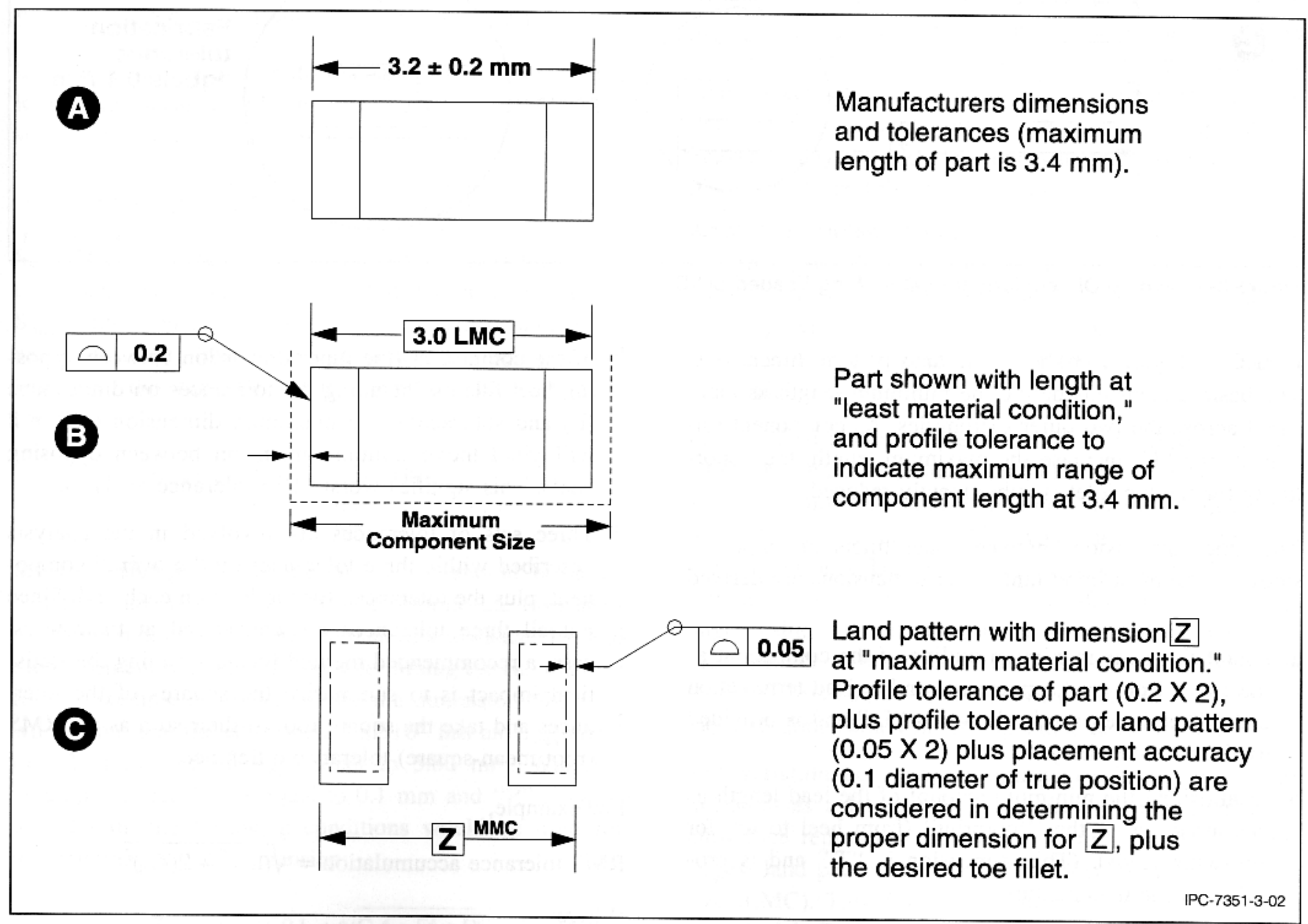



**Figure 3-2 Example of 3216 (1206) Capacitor Dimensioning for Optimum Solder Fillet Condition**

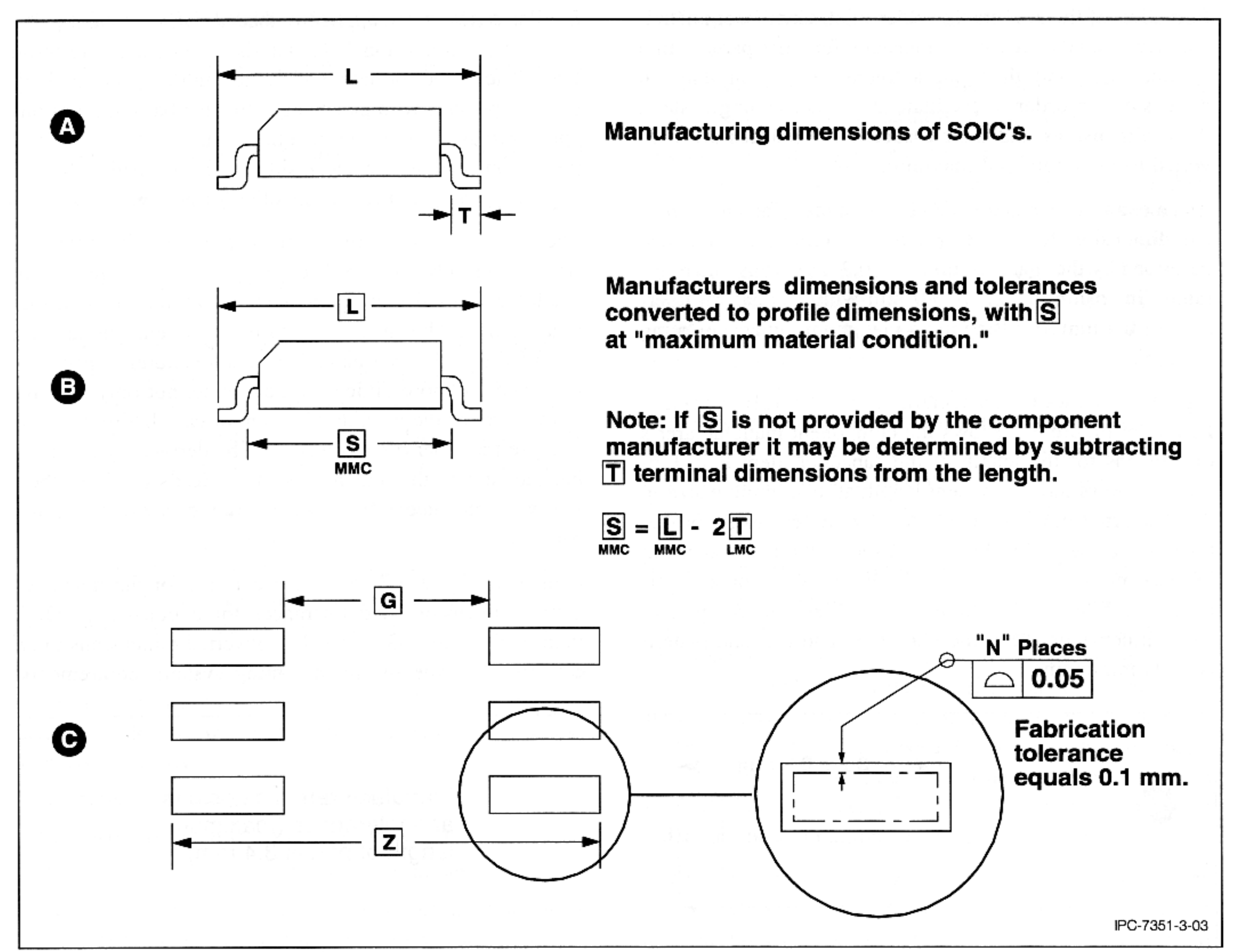



**Figure 3-3 Profile Dimensioning of Gull-Wing Leaded SOIC**

Item C in Figure 3-3 shows the land pattern dimensions. The basic dimensions define the minimum length as measured across the two outer extremities. As component tolerances for "L" increase the maximum length, the opportunity for the toe fillet is subsequently reduced.

The inner dimensions between heel fillets on opposing sides are the most important. Inner dimensions are derived by:

a. Establishing the maximum outline of the component as measured from lead termination end to lead termination end. (This dimension is shown as "L," and is provided by the manufacturer).

b. Establishing the minimum amount of the lead length as measured across the "footprint" (from heel to toe for gull-wing leads). (This dimension is "T," and is provided by the manufacturer).

c. Subtracting twice the minimum lead length of (T) from the maximum overall component length of (L) to arrive at the maximum length inside the leads across the length of the component (the inner dimension between opposing heel fillets). Including the tolerances on dimensions (L) and subtracting the maximum dimension of T x 2 will yield the minimum dimension between opposing heels. This signifies worst- case tolerance analysis.

d. Three sets of tolerances are involved in the analysis described within three tolerances on the overall component, plus the tolerances for the lead on each end. Since not all three tolerances are considered at their worst case, a recommended method for determining the statistical impact is to summarize the squares of the tolerances and take the square root of their sum as the RMS (root-mean-square) tolerance difference.

For example,

$$\text{RMS tolerance accumulation} = \sqrt{(L_{tol})^2 + 2(T_{tol})^2}$$

Where:

$L_{tol} = L_{max} - L_{min}$
$T_{tol} = T_{max} - T_{min}$

tol = tolerance
max = maximum
min = minimum

As an example, the SOIC with 16 leads has the following limits for the "L" (component length) and "T" (terminal length) dimensions:

$L_{min}$ = 5.8 mm, $L_{max}$ = 6.2 mm
$L_{tol} = L_{max} - L_{min}$ = 6.2 mm - 5.8 mm = 0.4 mm
$T_{min}$ = 0.4 mm, $T_{max}$ = 1.27 mm
$T_{tol} = T_{max} - T_{min}$ = 1.27 mm - 0.4 mm = 0.87 mm

Therefore, the calculations for "S" minimum and maximum dimensions are as follows:

$S_{min} = L_{min} - 2T_{max}$ = 5.8 mm - 2 (1.27 mm) = 3.26 mm
$S_{max} = L_{max} - 2T_{min}$ = 6.2 mm - 2 (0.4 mm) = 5.40 mm
$S_{tol} = S_{max} - S_{min}$ = 5.4 mm - 3.26 mm = 2.14 mm

The difference between $S_{min}$ and $S_{max}$ is 2.14 mm, which is probably a larger tolerance range than the actual range within which these components are manufactured. This worst-case scenario for the tolerance range for "S" can also be calculated by adding the tolerances for the component length and the two terminals:

$S_{tol} = L_{tol} + 2T_{tol}$ = 0.4 mm + 2 (0.87 mm) = 2.14 mm

In order to arrive at a more realistic tolerance range, the RMS value is calculated using the tolerances on the dimensions involved ("L" and "T"):

$$S_{tol}\,(RMS) = \sqrt{(L_{tol})^2 + 2(T_{tol})^2} = \sqrt{0.4^2 + 2(0.87)^2} = 1.29\text{ mm}$$

$S_{tol}$ (RMS) is added to $S_{min}$ to arrive at a maximum "S" dimension. This technique is used so that a more realistic $S_{max}$ dimension is used in the land pattern equations for calculating $G_{min}$ (minimum land pattern gap between heel fillets). In this example, the following calculation is used for $S_{max}$:

$$\begin{aligned} S_{max}\,(RMS) &= S_{min} + S_{tol}\,(RMS) \\ &= 3.26\text{ mm} + 1.29\text{ mm} \\ &= 4.55\text{ mm} \end{aligned}$$

**3.1.1.1 Solving for Dimension "Z"** It should be noted that there are various options to determine the tolerances for the component (C), the fabrication allowance (F), and the placement tolerance (P). In determining the calculations for the example in Figure 3-3 for the dimension "Z," one would note that the component "SO16" has an $L_{max}$ equal to 6.20 mm, and an $L_{min}$ equal to 5.80 mm. With the assumption that "F" is equal to 0.1 mm and "P" is equal to 0.2 mm, the following conditions would be used for determining the "Z" dimension:

$$Z_{max} = L_{min} + 2J_T + \sqrt{C_L{}^2 + F^2 + P^2}$$

$$Z_{max} = 6.20\text{ mm} + 2J_T + \sqrt{0.4^2 + 0.1^2 + 0.2^2}$$

In the above example, the two joints should be rounded to a realistic number. Normally a total Z dimension of 7.0 mm would be acceptable for a density level B land pattern providing a 0.4 mm land protrusion at either end of the SO16 component.

**3.1.2 Land Tolerancing** Profile tolerancing is used for lands in a manner similar to that of the components. All tolerances for lands are intended to provide a projected land pattern with individual lands at maximum size. Unilateral tolerances are intended to reduce the land size and thus result in a lesser area for solder joint formation. In order to facilitate companion dimension systems, the land pattern is dimensioned across outer and inner extremities.

The dimensioning concept in this standard uses limiting dimensions and geometric tolerancing to describe the allowable maximum and minimum dimensions of the land pattern. When lands are at their maximum size, the result may be a minimum acceptable space between lands; conversely when lands are at their minimum size, the result may be a minimum acceptable land pattern necessary to achieve the minimum required land protrusion. These thresholds allow for gauging of the land pattern for go/no-go conditions. The whole concept of the dimensioning system described in this document is based on these principles and extends to component mounting dimensions, land pattern dimensions, positioning dimensions, etc., so that the requirements may be examined using optical gauges at any time in the process in order to insure compliance with the tolerance analysis (see Table 3-16).

**3.1.3 Fabrication Allowances** Figure 3-3 shows the land pattern for an SOIC with gull-wing leads intended to be a companion to the chip component dimensioning concepts shown previously in Figure 3-2. The basic "L" dimension is across the outer extremities of the component lead or terminal.

For the land pattern, dimension "Z" is at maximum size, while the inner extremities (dimension "G") are dimensioned at minimum size. Unilateral tolerances decreased the basic dimension for "Z" while increasing the basic "G" dimension. This action results in a reduced land pattern at Least Material Condition (LMC). Thus, processing target values should be as close as possible to the basic "Z" and "G" dimensions at Maximum Material Condition (MMC). This concept also holds true for the width (X) of the land dimension which is specified at maximum size.

The variation between the dimensions Z, G, and X are indicated as a fabrication allowance (F). This fabrication allowance represents the maximum variation between the largest land pattern size (MMC) and the least land pattern size (LMC). This does not include material movement as described in Table 3-16, which is included in the assembly tolerancing since machine vision capability revaluates the true position of the land pattern.

**3.1.4 Assembly Tolerancing** Another part of the equation is the assembly variation defined by the letter "P." This variation represents the location of the component in relation to its true position as defined by the design. The term diameter of true position (DTP) is used to describe this variation and is a single number that can be used in the dimensional tolerance analysis.

As an example, for establishing the target heel protrusion dimensions of the example shown in Figure 3-3, the following conditions would be true:

Where:

J is 0.5 mm (target heel fillet).
C is $S_{tol}$ (RMS) = 1.29 mm (see previous calculations from component dimensions).
F is 0.1 mm (assumed fabrication tolerance).
P is 0.05 mm (assumed assembly equipment placement tolerance).

Therefore:

$$G_{min} = 4.55\text{ mm} - 2(0.5\text{ mm}) - \sqrt{(1.29)^2 + (0.1)^2 + (0.05)^2}$$
$$= 2.25\text{ mm}$$

Another major condition for multiple-leaded components that must be considered in land pattern design is lead, termination, or castellation pitch. The pitch describes the basic dimension of the spacing of one component lead termination or castellation to its adjacent counterpart(s). No tolerance is assigned to pitch in the profile dimensioning concept. Differences in pitch are included in the width dimensions of the lead, termination, or castellation which are dimensioned as basic at the minimum size.

**3.1.5 Dimension and Tolerance Analysis** In analysing the design of a component/land pattern system, several things come into play, including the size and position tolerances of the component lead or termination, the tolerances of the land pattern, and the placement accuracy of the man/machine to center the part to the land pattern. The result is the land area available for a solder joint that provides a proper formation of a toe, heel, or side fillet.

System equations have been developed for chip components and multiple leaded parts. These concepts assume that the target values of parts and land patterns are maximized to reflect solder joint formation (i.e., outer dimensions of components at minimum size with outer dimensions of land patterns at maximum size). The equations use the following symbols:

C is the unilateral profile tolerance(s) for the component.
F is the unilateral profile tolerance(s) for the board land. pattern
P is the diameter of true position placement accuracy to the center of the land pattern.

With the assumption that a particular solder joint or solder volume is desired for every component, some methods use the worst-case criteria for determining a dimension. This would require that "C," "F," and "P" be added to the minimum dimension of the component length plus the solder joint requirements, in order to determine the maximum dimension of the outer land pattern.

Experience shows that the worst-case analysis is not always necessary; therefore statistical methods are used by taking the square root of the sum of the squares of the tolerances. This method assumes that all features will not reach their worst case. The equations for determining component land pattern requirements are as follows:

$$Z_{max} = L_{min} + 2J_T + \sqrt{C_L{}^2 + F^2 + P^2}$$

$$G_{min} = S_{max} - 2J_H - \sqrt{C_S{}^2 + F^2 + P^2}$$

$$X_{max} = W_{min} + 2J_S + \sqrt{C_W{}^2 + F^2 + P^2}$$

Where:

Z is the overall length of land pattern.
G is the distance between lands of the pattern.
X is the width of land pattern.
L is the overall length of component.
S is the distance between component terminations.
W is the width of the lead or termination.
J is the desired dimension of solder fillet or land protrusion.
- $J_T$ is the solder fillet or land protrusion at toe.
- $J_H$ is the solder fillet or land protrusion at heel.
- $J_S$ is the solder fillet or land protrusion at side.

C is the component tolerances.
- $C_L$ is the tolerance on component length.
- $C_S$ is the tolerance on distance between component terminations.
- $C_W$ is the tolerance on the lead width.

F is the printed board fabrication (land pattern geometric) tolerances.
P is the part placement tolerance (placement equipment accuracy).

The formula (the square root of the sum of the squares) is identical for both toe and heel solder joint formation (different tolerances are used, however). However, the desired solder joint dimension and the square root of the sum of the squares are added for outer land pattern dimensions and subtracted for inner land pattern dimensions. The result provides the final land pattern dimensions Z, G, and X.

The same concept is true for chip, multiple leaded or leadless components. Additionally, pitch with lead-to-land overlap (M) can be evaluated as well as the space (N) to reflect the clearance between a lead, termination, or castellation and the adjacent land(s). These latter values are not used in the equations to determine the land pattern sizes, but may be used to limit lead-to-adjacent land proximity and to adjust lead-to-land overlap (see Figure 3-4).

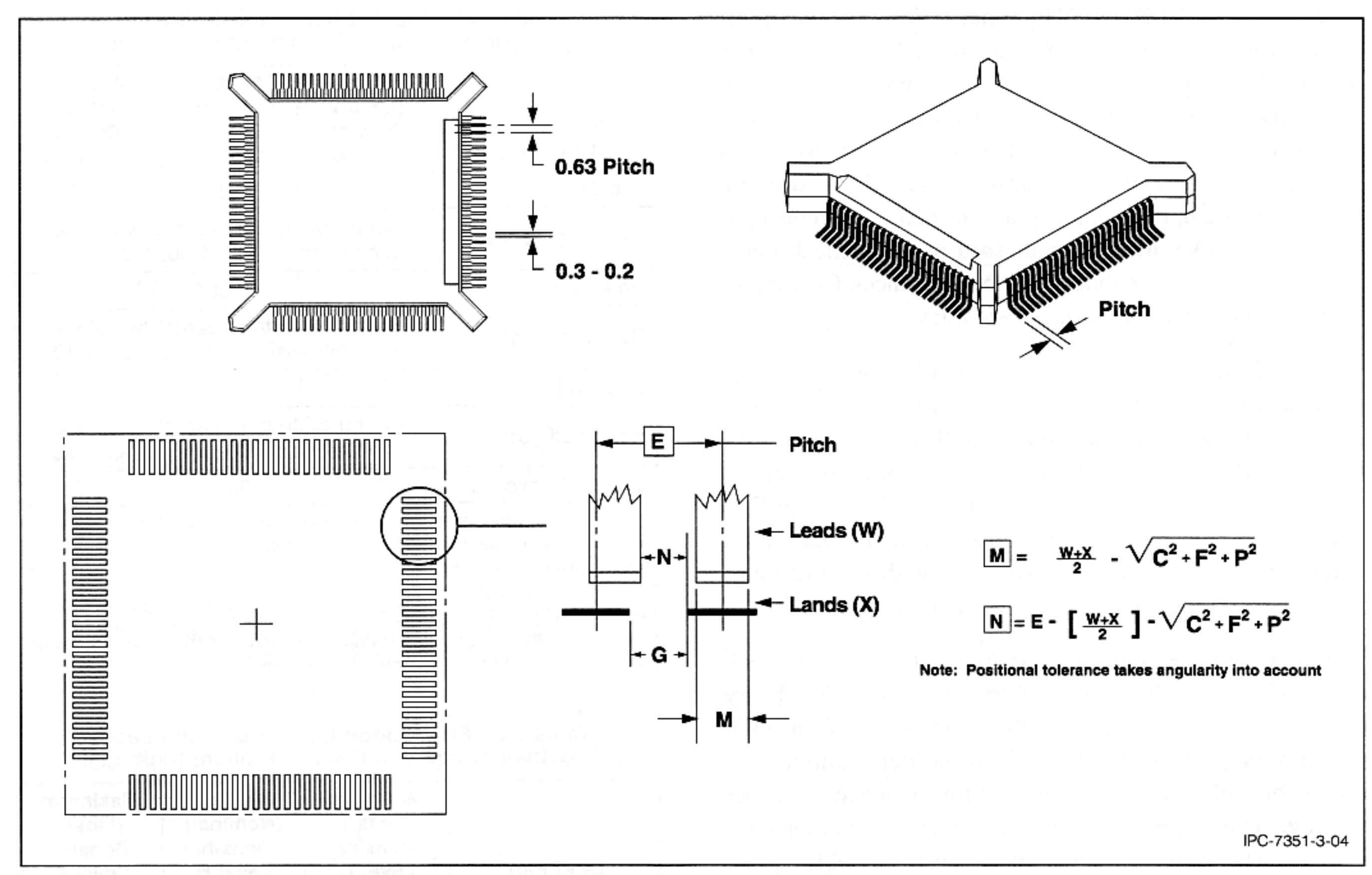



**Figure 3-4 Pitch for Multiple Leaded Components**

The equations for determining if the clearance "N" or the attachment overlap "M" are sufficient is as follows:

$$M = \left[\frac{W+X}{2}\right] - \sqrt{C^2 + F^2 + P^2}$$

$$N = E - \left[\frac{W+X}{2}\right] + \sqrt{C^2 + F^2 + P^2}$$

**3.1.5.1 Tolerance and Solder Joint Analysis** The following tolerance concepts are used to determine the land patterns for electronic components. These concepts are detailed in Table 3-1 and reflect the tolerances on the component, the tolerances on the land pattern (on the interconnecting substrate), and the accuracy of the equipment used for placing components.

Solder joint minimums are shown for toe, heel and side fillets. These conditions are minimums, since the equations in 3.1 address the component, board, and placement accuracy tolerances (sum of the squares). The minimum solder joint or land protrusion is increased by the amount that the tolerance variation does not use up. The courtyard excess is added to the maximum dimension that the land pattern or component occupies. The courtyard excess number is added to each side of the dimension in question. It is intended that this addition provides sufficient room for electrical and physical clearance between components and/or land patterns. Since the total of all the number calculations may not result in a reasonable numerical equivalent, a suggested round-off (up or down) feature has been added to the tables to identify a rounding up value for the final number to be used in the design.

**Table 3-1 Tolerance Analysis Elements for Chip Devices**

| Tolerance Element | Detailed Description |
|---|---|
| Component Tolerance | The difference between the MMC and the LMC of each component dimension, length, width and distance between terminations or leads. This number is the "C" tolerance in the equations. |
| Board Tolerance | The difference between the MMC and the LMC of each land pattern dimension. This number is the "F" tolerance in the equations. |
| Positional Accuracy | Positional accuracy is defined as diameter of true position (DTP). This is the variation of the part centroid related to the land pattern theoretical center (includes feature location tolerance from Table 3-17). |
| Toe Fillet | The land protrusion beyond the lead or termination extremities (see Tables 3-2 through 3-14). |
| Heel Fillet | The land protrusion beyond the internal lead or termination dimensions (see Tables 3-2 through 3-14). |
| Side Fillet Width | The land protrusion to either side of the lead or termination (see Tables 3-2 through 3-14). |

The IPC-7351 Library Documentation spreadsheets included with this standard provide an analysis of tolerance assumptions and resultant solder joints based on the finished land pattern dimensions. Tolerances for component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration. These tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication and placement accuracy.

Individual tolerances for fabrication ("F") and component placement equipment accuracy ("P") are assumed to be as given in spreadsheet documentation. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges ($C_L$, $C_S$, and $C_W$) are derived by subtracting minimum from maximum dimensions given. The user may also modify these numbers, based on experience with their suppliers.

The dimensions for minimum solder fillets at the toe, heel, or side ($J_T$, $J_H$, $J_S$) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the library documentation spreadsheets usually provide for a positive solder fillet. Nevertheless, if the user of any of the three land pattern geometry variations desires a more robust process condition for placement and soldering equipment, individual elements of the analysis may be changed to new and desired dimensional conditions. This includes component, board or placement accuracy spread, as well as minimum solder joint or land protrusion expectation. In addition, this standard recognizes the need to have different goals for the solder fillet or land protrusion conditions.

Tables 3-2 through 3-14 indicate the principles used for the three goals established by this standard. The tables reflect maximum (most), median (nominal) and minimum (least) material conditions for the land protrusions used to develop land patterns for surface mounting various lead or terminations of components. Unless otherwise indicated, the IPC-7351 identifies all three goals as Density Levels A, B, or C.

**Table 3-2 Flat Ribbon L and Gull-Wing Leads (greater than 0.625 mm pitch) (unit: mm)**

| Lead Part | Minimum (Least) Density Level C | Median (Nominal) Density Level B | Maximum (Most) Density Level A |
|---|---|---|---|
| Toe ($J_T$) | 0.15 | 0.35 | 0.55 |
| Round-off factor | Round off to the nearest two place even decimal, i.e., 1.00, 1.20, 1.40 | | |
| Heel ($J_H$)[1] | 0.25 | 0.35 | 0.45 |
| Round-off factor | Round off to the nearest two place even decimal, i.e., 1.00, 1.20, 1.40 | | |
| Side ($J_S$) | 0.01 | 0.03 | 0.05 |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 | | |
| Courtyard excess | 0.1 | 0.25 | 0.5 |

1. For gullwing components where dimension Smin is less than or equal to dimension Amax, use the following heel fillet goals:
Density Level C - 0.05 mm
Density Level B - 0.15 mm
Density Level A - 0.25 mm
**Note:** This does not apply to gullwing components where the lead terminals have a tolerance T1 that is greater than 0.5 mm.

**Table 3-3 Flat Ribbon L and Gull-Wing Leads (less than or equal to 0.625 mm pitch) (unit: mm)**

| Lead Part | Minimum (Least) Density Level C | Median (Nominal) Density Level B | Maximum (Most) Density Level A |
|---|---|---|---|
| Toe ($J_T$) | 0.15 | 0.35 | 0.55 |
| Round-off factor | Round off to the nearest two place even decimal, i.e., 1.00, 1.20, 1.40 | | |
| Heel ($J_H$)[1] | 0.25 | 0.35 | 0.45 |
| Round-off factor | Round off to the nearest one place decimal, i.e., 1.0, 1.1, 1.2, 1.3 | | |
| Side ($J_S$) | -0.04 | -0.02 | 0.01 |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 | | |
| Courtyard excess | 0.1 | 0.25 | 0.5 |

1. For gullwing components where dimension Smin is less than or equal to dimension Amax, use the following heel fillet goals:
Density Level C - 0.05 mm
Density Level B - 0.15 mm
Density Level A - 0.25 mm
**Note:** This does not apply to gullwing components where the lead terminals have a tolerance T1 that is greater than 0.5 mm.

**3.1.5.2 Component Dimensions** Illustrations of component dimensions in each library documentation spreadsheet are accompanied by a table of figures for each of the different part numbers, as taken from multinational component standards organizations. The standards organizations provide many more dimensions to define the requirements for manufacturing the specific components in a family class; only those dimensions that are necessary for land pattern development are repeated within the library documentation spreadsheets. At times, the component tolerances or component gauge requirements do not necessarily reflect the exact tolerance on a manufacturer's data sheet. Component dimensions are provided according to the concepts of maximum and least materials condition (MMC and LMC). Both conditions are presented in the tables within the library documentation spreadsheets. The component manufacturers may not always dimension their components in accordance with the limits shown in the tables. However, these limits may be used as criteria for go/no-go acceptance of the component. The LMC dimensions of the figure are those that have been used in the equations described in 3.1 for determining the recommended land pattern.

**Table 3-4 J Leads (unit: mm)**

| Lead Part | Minimum (Least) Density Level C | Median (Nominal) Density Level B | Maximum (Most) Density Level A |
|---|---|---|---|
| Heel (to find Z dim) ($J_H$) | 0.15 | 0.35 | 0.55 |
| Round-off factor | Round off to the nearest two place even decimal, i.e., 1.00, 1.20, 1.40 | | |
| Toe (to find G dim) ($J_T$) | -0.30 | -0.20 | -0.10 |
| Round-off factor | Round off to the nearest two place even decimal, i.e., 1.00, 1.20, 1.40 | | |
| Side ($J_S$) | 0.01 | 0.03 | 0.05 |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 | | |
| Courtyard excess | 0.1 | 0.25 | 0.5 |

**Table 3-5 Rectangular or Square-End Components (Capacitors and Resistors) Equal to or Larger than 1608 (0603) (unit: mm)**

| Lead Part | Minimum (Least) Density Level C | Median (Nominal) Density Level B | Maximum (Most) Density Level A |
|---|---|---|---|
| Toe ($J_T$) | 0.15 | 0.35 | 0.55 |
| Round-off factor | Round off to the nearest two place even decimal, i.e., 1.00, 1.20, 1.40 | | |
| Heel ($J_H$) | -0.05 | -0.05 | -0.05 |
| Round-off factor | Round off to the nearest two place even decimal, i.e., 1.00, 1.20, 1.40 | | |
| Side ($J_s$) | -0.05 | 0.00 | 0.05 |
| Round-off factor | Round off to the nearest one place decimal, i.e., 1.0, 1.1, 1.2, 1.3 | | |
| Courtyard excess | 0.1 | 0.25 | 0.5 |

**Table 3-6 Rectangular or Square-End Components (Capacitors and Resistors) Smaller than 1608 (0603) (unit: mm)**

| Lead Part | Minimum (Least) Density Level C | Median (Nominal) Density Level B | Maximum (Most) Density Level A |
|---|---|---|---|
| Toe ($J_T$) | 0.00 | 0.10 | 0.20 |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 | | |
| Heel ($J_H$) | -0.05 | -0.05 | -0.05 |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 | | |
| Side ($J_S$) | 0.00 | 0.00 | 0.05 |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 | | |
| Courtyard excess | 0.1 | 0.15 | 0.20 |

**Table 3-7 Cylindrical End Cap Terminations (MELF) (unit: mm)x**

| Lead Part | Minimum (Least) Density Level C | Median (Nominal) Density Level B | Maximum (Most) Density Level A |
|---|---|---|---|
| Toe ($J_T$) | 0.2 | 0.4 | 0.6 |
| Round-off factor | Round off to the nearest two place even decimal, i.e., 1.00, 1.20, 1.40 | | |
| Heel ($J_H$) | 0.02 | 0.1 | 0.2 |
| Round-off factor | Round off to the nearest two place even decimal, i.e., 1.00, 1.20, 1.40 | | |
| Side ($J_S$) | 0.01 | 0.05 | 0.1 |
| Round-off factor | Round off to the nearest one place decimal, i.e., 1.0, 1.1, 1.2, 1.3 | | |
| Courtyard excess | 0.1 | 0.25 | 0.5 |

**Table 3-8 Bottom Only Terminations (unit: mm)**

| Lead Part | Minimum (Least) Density Level C | Median (Nominal) Density Level B | Maximum (Most) Density Level A |
|---|---|---|---|
| Toe ($J_T$) | 0.15 | 0.35 | 0.55 |
| Round-off factor | Round off to the nearest two place even decimal, i.e., 1.00, 1.20, 1.40 | | |
| Heel ($J_H$) | 0.25 | 0.35 | 0.45 |
| Round-off factor | Round off to the nearest one place decimal, i.e., 1.0, 1.1, 1.2, 1.3 | | |
| Side ($J_S$) | 0.01 | 0.03 | 0.08 |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 | | |
| Courtyard excess | 0.1 | 0.25 | 0.5 |

**Table 3-9 Leadless Chip Carrier with Castellated Terminations (unit: mm)**

| Lead part | Minimum (Least) Density Level C | Median (Nominal) Density Level B | Maximum (Most) Density Level A |
|---|---|---|---|
| Heel ($J_H$) (to find Z dim) | 0.45 | 0.55 | 0.65 |
| Round-off factor | Round off to the nearest two place even decimal, i.e., 1.00, 1.20, 1.40 | | |
| Toe ($J_T$) (to find G dim) | 0.05 | 0.15 | 0.25 |
| Round-off factor | Round off to the nearest two place even decimal, i.e., 1.00, 1.20, 1.40 | | |
| Side ($J_S$) | -0.15 | -0.05 | 0.05 |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 | | |
| Courtyard excess | 0.1 | 0.25 | 0.5 |

**Table 3-10 Butt Joints (unit: mm)**

| Lead Part | Minimum (Least) Density Level C | Median (Nominal) Density Level B | Maximum (Most) Density Level A |
|---|---|---|---|
| Toe ($J_T$) | 0.6 | 0.8 | 1.0 |
| Round-off factor | Round off to the nearest two place even decimal, i.e., 1.00, 1.20, 1.40 | | |
| Heel ($J_H$) | 0.6 | 0.8 | 1.0 |
| Round-off factor | Round off to the nearest one place decimal, i.e., 1.0, 1.1, 1.2, 1.3 | | |
| Side ($J_S$) | 0.1 | 0.2 | 0.3 |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 | | |
| Courtyard excess | 0.2 | 0.8 | 1.5 |

**Table 3-11 Inward Flat Ribbon L and Gull-Wing Leads (Tantalum Capacitors) (unit: mm)**

| Lead Part | Minimum (Least) Density Level C | Median (Nominal) Density Level B | Maximum (Most) Density Level A |
|---|---|---|---|
| Toe (to find G dim) ($J_T$) | 0.07 | 0.15 | 0.25 |
| Round-off factor | Round off to the nearest two place even decimal, i.e., 1.00, 1.20, 1.40 | | |
| Heel (to find Z dim) ($J_H$) | 0.2 | 0.5 | 0.8 |
| Round-off factor | Round off to the nearest two place even decimal, i.e., 1.00, 1.20, 1.40 | | |
| Side ($J_S$) | -0.10 | -0.05 | 0.01 |
| Round-off factor | Round off to the nearest one place decimal, i.e., 1.0, 1.1, 1.2, 1.3 | | |
| Courtyard excess | 0.1 | 0.25 | 0.5 |

**Table 3-12 Flat Lug Leads (unit: mm)**

| Lead Part | Minimum (Least) Density Level C | Median (Nominal) Density Level B | Maximum (Most) Density Level A |
|---|---|---|---|
| Toe ($J_T$) | 0.15 | 0.35 | 0.55 |
| Round-off factor | Round off to the nearest two place even decimal, i.e., 1.00, 1.20, 1.40 | | |
| Heel ($J_H$) | 0.25 | 0.35 | 0.45 |
| Round-off factor | Round off to the nearest one place decimal, i.e., 1.0, 1.1, 1.2, 1.3 | | |
| Side ($J_S$) | -0.04 | 0.01 | 0.05 |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 | | |
| Courtyard excess* | 0.1 | 0.25 | 0.5 |

* Depends on thermal requirements.

**Table 3-13 Flat, No Lead (unit: mm)**

| Lead Part | Minimum (Least) Density Level C | Median (Nominal) Density Level B | Maximum (Most) Density Level A |
|---|---|---|---|
| Toe ($J_T$) | 0.20 | 0.30 | 0.40 |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 | | |
| Heel ($J_H$) | 0.00 | 0.00 | 0.00 |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 | | |
| Side ($J_S$) | -0.04 | -0.04 | -0.04 |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 | | |
| Courtyard excess | 0.1 | 0.25 | 0.5 |

**Note:** The rationale for the relatively large negative heel stems from the tolerances for the lead lengths as also being relatively large. In order to maintain a minimum clearance of 0.20 mm to the thermal tab it becomes necessary to trim the heel by -0.2 mm. Without a thermal tab the heel can usually be increased to as much as 0.50 mm.

**Table 3-14 Small Outline (SO), No-Lead (unit: mm)**

| Lead Part | Minimum Level C | Median Level B | Maximum Level A |
|---|---|---|---|
| Toe ($J_T$) | 0.20 | 0.30 | 0.40 |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 | | |
| Heel ($J_H$) | 0.00 | 0.00 | 0.00 |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 | | |
| Side ($J_S$) | -0.04 | -0.04 | -0.04 |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 | | |
| Courtyard excess | 0.1 | 0.25 | 0.5 |

**Note:** With a thermal tab the heel can usually be increased to as much as 0.1 mm.

Dimensions that have had their tolerance spread reduced are so indicated in the tables. Parts that are available with shape characteristics or tolerance limits that fall outside the recommended norms require land patterns that must be altered slightly from those presented.

Users of these specialized parts are encouraged to develop their own land patterns which then become unique to a specific component vendor part. A dimensioning system with specific equations has been provided to facilitate unique land pattern development or enhance process usage.

**3.1.5.3 Land Pattern Dimensions** Land pattern dimensions are provided in the sectional standards according to the concepts of maximum material conditions (MMC).

Sometimes a dimension is presented as a minimum distance. This occurs when defining a space(s) that exists between lands at MMC. The printed board manufacturer may not always inspect the board in accordance with the limit concepts shown in the table. However, these limits may be used as the criteria for go/no-go acceptance of the printed board land pattern. The dimensions shown in each table are those that have been used in the equations described in 3.1 for determining the recommended land patterns. The maximum material condition for each land pattern analysis level describes the most robust joint or land protrusion for that level land pattern.

**3.1.5.4 Courtyard Determination** The courtyard of any land pattern is the smallest area that provides a minimum electrical and mechanical clearance of both the component maximum boundary extremities and/or the land pattern maximum boundary extremities. The intent of the courtyard is to aid the designer in determining the minimum area occupied by the combination of component and land pattern. The information provided in Tables 3-2 through 3-14 is intended to relate to those excesses that should be added to the maximum dimension to derive the appropriate courtyard condition.

As an example, if a component was the major determining factor of the boundary condition, it would have the excess added to the dimensions. The same holds true for a land pattern that has the greater extremities. If either dimension were 14.5 mm, and the excess from tables 3-2 through 3-14 indicated an excess of 0.8 mm, the resulting courtyard would theoretically be 16.1 mm. The tables further define a round-up feature. If the round-up were recommended as being to the nearest 0.5 mm, the courtyard would become 16.5 mm.

It should be noted that 16.5 mm is a number that, when divided by 2 to obtain the component centroid, provides 2 decimal places to the right of the number. It therefore may be appropriate to keep this number in an even approximation such as 16.6 mm. This would provide 8.3 mm to either side of the center of the component to help designers position the component in relation to some grid or placement algorithm.

When manufacturing allowance must be considered in the design process the courtyard represents the starting point of the minimum area needed for the component and the land pattern. Manufacturing, assembly and testing representatives should assist in determining the additional room needed to accommodate placement, testing, modification and repair. This manufacturing allowance is usually dependent on the density and complexity of the product, and is not defined in this document. The manufacturing allowance is determined by application and manufacturing process requirements (see Figure 3-5).

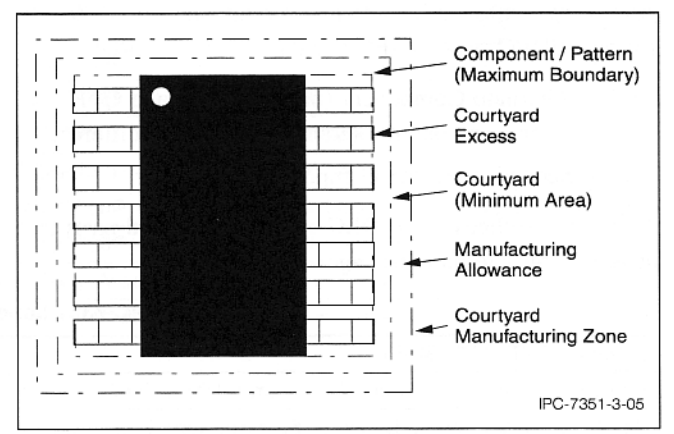



**Figure 3-5 Courtyard Boundary Area Condition**

**3.1.5.5 Land Pattern Naming Convention** The RLP (Registered Land Pattern) numbering scheme previously used in IPC-SM-782A has been replaced with an intelligent land pattern naming convention which will aid in the standardization of electronic schematic symbols for engineering.

Each land pattern in the IPC-7351 has received a name containing a prefix for the device type, a pin pitch, a nominal lead span corresponding to the "L" dimension (or a pair of nominal lead spans for components with termination leads on four sides), and a pin quantity. In the case of ball grid array (BGA) packages, the column and row numbers are given as there are no end termination lead spans. The purpose of the number is to aid in communication between engineering, design, and manufacturing. Specific syntax explanations include:

The + (plus sign) stands for "in addition to" (no space between the prefix and the body size).

The - (dash) is used to separate the pin qty.

The X (capital letter X) is used instead of the word "by" to separate two numbers such as height X width like "Quad Packages."

The suffix letters of L, M and N are reserved by IPC. The suffix letters "L," "M," and "N" have been reserved to signify when the land protrusion is at their minimum (least), maximum (most), or median (nominal) protrusion or use environment as follows:

M – Maximum (Most) Material Condition (Density Level A)

N – Median (Nominal) Material Condition (Density Level B)

L – Minimum (Least) Material Condition (Density Level C)

**Note:** Ball Grid Array (BGA) and Quad Flat No-Lead (QFN) packages do not receive a suffix of "L," "M" or "N" as they are only listed in the median (nominal) density level.

Additional suffixes for alternate components that do not follow JEDEC, EIA or IEC standards are as follows:

"A" – Alternate Component (used for SOP and QFP when component tolerance or height is different)

"B" – Second Alternate Component

Additional suffices for JEDEC and EIA Standard parts that have several alternate packages are as follows:

AA, AB, AC JEDEC or EIA Component Identifier (Used primarily on Chip Resistors, Inductors and Capacitors).

The naming conventions shown in Table 3-15 are subject to change as new component families are identified. The most current naming convention listing can be found on the IPC website (**www.ipc.org**) under "PCB Tools and Calculators.".

**Table 3-15 IPC-7351 Land Pattern Naming Convention**

| COMPONENT, CATEGORY | LAND PATTERN NAME |
|---|---|
| Ball Grid Array's, Inch Based (1.27 mm / 0.05 in Pitch) | **BGA127P** + Number of Pin Columns **X** Number of Pin Rows - Pin Qty |
| Ball Grid Array's, Metric Based (1.50 mm Pitch) | **BGA150P** + Number of Pin Columns **X** Number of Pin Rows - Pin Qty |
| Ball Grid Array's, Metric Based (1.00 mm Pitch) | **BGA100P** + Number of Pin Columns **X** Number of Pin Rows - Pin Qty |
| Ball Grid Array's, Metric Based (0.80 mm Pitch) | **BGA80P** + Number of Pin Columns **X** Number of Pin Rows - Pin Qty |
| Ball Grid Array's, Metric Based (0.75 mm Pitch) | **BGA75P** + Number of Pin Columns **X** Number of Pin Rows - Pin Qty |
| Ball Grid Array's, Metric Based (0.65 mm Pitch) | **BGA65P** + Number of Pin Columns **X** Number of Pin Rows - Pin Qty |
| Ball Grid Array's, Metric Based (0.50 mm Pitch) | **BGA50P** + Number of Pin Columns **X** Number of Pin Rows - Pin Qty |
| Ball Grid Array's w/Staggered Pins (1.27 mm Pitch) | **SBGA127P** + Number of Pin Columns **X** Number of Pin Rows - Pin Qty |
| Capacitors, Chip, Array | **CAPCA** + Pitch P + Body Width X Body Length in Metric - Pin Qty |
| Capacitors, Chip, Polarized | **CAPCP** + Body Size in Metric |
| Capacitors, Chip, Nonpolarized | **CAPC** + Body Size in Metric |
| Capacitors, Chip, Wire Rectangle | **CAPCWR** + Body Size in Metric |
| Capacitors, Molded, Nonpolarized | **CAPM** + Body Size in Metric |
| Capacitors, Molded, Polarized | **CAPMP** + Body Size in Metric |
| Capacitors, Aluminum Electrolytic | **CAPAE** + Base Body Width (**W**) + Height (**H**) |
| Ceramic Flat Packages | **CFP127P** + Lead Span Nominal - Pin Qty |
| Column Grid Array's | **CGA** + Number of Pin Columns **X** Number of Pin Rows - Pin Qty |
| Diodes, Molded (JEDEC Standard Package) | **DIOM** + Body Size in Metric |
| Diodes, MELF | **DIOMELF** + Body Size in Metric |
| Inductors, Chip | **INDC** + Body Size in Metric |
| Inductors, Chip, Array | **INDCA** + Pitch P + Body Width X Body Length in Metric - Pin Qty |
| Inductors, Molded | **INDM** + Body Size in Metric |
| Inductors, Precision Wire Wound | **INDP** + Body Size in Metric |
| Plastic Leaded Chip Carriers Square (JEDEC Standard Package) | **PLCC** - Pin Qty |
| Plastic Leaded Chip Carriers Rectangular (JEDEC Standard Package) | **PLCCR** - Pin Qty |
| Plastic Leaded Chip Carrier Sockets Square | **PLCCS** - Pin Qty |
| Plastic Leaded Chip Carrier Sockets Rectangular | **PLCCRS** - Pin Qty |
| Plastic Quad Flat Packages, 0.635 mm Pitch, Pin 1 Side | **PQFPS** - Pin Qty |
| Plastic Quad Flat Packages, 0.635 mm Pitch, Pin 1 Center | **PQFPC** - Pin Qty |
| Bumper Quad Flat Packages, 0.635 mm Pitch, Pin 1 Side | **BQFPS** - Pin Qty |
| Bumper Quad Flat Packages, 0.635 mm Pitch, Pin 1 Center | **BQFPC** - Pin Qty |
| Quad Flat Packages, 1.00 mm Pitch | **QFP100P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty |
| Quad Flat Packages, 0.80 mm Pitch | **QFP80P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty |
| Quad Flat Packages, 0.65 mm Pitch | **QFP65P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty |
| Shrink Quad Flat Packages, 0.50 mm Pitch | **SQFP50P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty |
| Shrink Quad Flat Packages, 0.40 mm Pitch | **SQFP40P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty |
| Shrink Quad Flat Packages, 0.30 mm Pitch | **SQFP30P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty |
| Thin Quad Flat Packages, 0.80 mm Pitch, Height ≤ 1.60 mm | **TQFP80P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty |
| Thin Quad Flat Packages, 0.65 mm Pitch, Height ≤ 1.60 mm | **TQFP65P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty |

| COMPONENT, CATEGORY | LAND PATTERN NAME |
|---|---|
| Thin Quad Flat Packages, 0.50 mm Pitch, Height ≤ 1.60 mm | **TSQFP50P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty |
| Thin Quad Flat Packages, 0.40 mm Pitch, Height ≤ 1.60 mm | **TSQFP40P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty |
| Thin Quad Flat Packages, 0.30 mm Pitch, Height ≤ 1.60 mm | **TSQFP30P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty |
| Ceramic Quad Flat Packages, 1.27 mm Pitch | **CQFP127P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty |
| Ceramic Quad Flat Packages, 0.80 mm Pitch | **CQFP80P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty |
| Ceramic Quad Flat Packages, 0.635 mm Pitch | **CQFP63P** + Lead Span L1 **X** Lead Span L2 Nominal - Pin Qty |
| Quad Flat No Lead Packages 0.80 mm Pitch | **QFN80P** - Body Width **X** Body Length in Metric - Pin Qty + Thermal Pad |
| Quad Flat No Lead Packages 0.65 mm Pitch | **QFN65P** - Body Width **X** Body Length in Metric - Pin Qty + Thermal Pad |
| Quad Flat No Lead Packages 0.50 mm Pitch | **QFN50P** - Body Width **X** Body Length in Metric - Pin Qty + Thermal Pad |
| Quad Flat No Lead Packages 0.40 mm Pitch | **QFN40P** - Body Width **X** Body Length in Metric - Pin Qty + Thermal Pad |
| Quad Leadless Ceramic Chip Carriers (JEDEC Standard Package) | **LCC** + Body Width **X** Body Length in Metric - Pin Qty |
| Quad Leadless Ceramic Chip Carriers (Pin 1 on Side) | **LCCS** + Body Width **X** Body Length in Metric - Pin Qty |
| Quad Bottom Chip Carrier (JEDEC MO-217B) | **QBCC** + Body Width **X** Body Length in Metric - Pin Qty |
| Resistors, Chip | **RESC** + Body Size in Metric |
| Resistors, Chip, Array | **RESCA** + Pitch P + Body Width X Body Length in Metric - Pin Qty |
| Resistors, Molded | **RESM** + Body Size in Metric |
| Resistors, MELF | **RESMELF** + Body Size in Metric |
| Small Outline IC, J-Leaded 300, 350, 400, 450 mil Body Width (Pitch 1.27 mm) | **SOJ127P** + Lead Span Nominal - Pin Qty |
| Small Outline IC, J-Leaded (Pitch 0.65 mm) | **SOJ65P** + Lead Span Nominal - Pin Qty |
| Small Outline Integrated Circuit, 1.27 mm Pitch (Standard 50 mil Pitch SOICs) | **SOIC127P** + Lead Span Nominal - Pin Qty |
| Small Outline Packages, 1.27 mm Pitch (Nonstandard 50 mil Pitch SOICs) | **SOP127P** + Lead Span Nominal - Pin Qty |
| Small Outline Packages, 1.00 mm Pitch | **SOP100P** + Lead Span Nominal - Pin Qty |
| Small Outline Packages, 0.80 mm Pitch | **SOP80P** + Lead Span Nominal - Pin Qty |
| Small Outline Packages, 0.65 mm Pitch | **SOP65P** + Lead Span Nominal - Pin Qty |
| Small Outline Packages, 0.635 mm Pitch | **SOP63** + Lead Span Nominal - Pin Qty |
| Shrink Small Outline Packages, 0.50 mm Pitch | **SSOP50P** + Lead Span Nominal - Pin Qty |
| Shrink Small Outline Packages, 0.40 mm Pitch | **SSOP40P** + Lead Span Nominal - Pin Qty |
| Shrink Small Outline Packages, 0.30 mm Pitch | **SSOP30P** + Lead Span Nominal - Pin Qty |
| Thin Small Outline Packages, Height is ≤ 1.60 mm, 1.27 mm Pitch | **TSOP127P** + Lead Span Nominal - Pin Qty |
| Thin Small Outline Packages, Height is ≤ 1.60 mm, 1.00 mm Pitch | **TSOP100P** + Lead Span Nominal - Pin Qty |
| Thin Small Outline Packages, Height is ≤ 1.60 mm, 0.80 mm Pitch | **TSOP80P** + Lead Span Nominal - Pin Qty |
| Thin Small Outline Packages, Height is ≤ 1.60 mm, 0.65 mm Pitch | **TSOP65P** + Lead Span Nominal - Pin Qty |
| Thin Shrink Small Outline Packages, Height is ≤ 1.60 mm, 0.55 mm Pitch | **TSSOP55P** + Lead Span Nominal - Pin Qty |
| Thin Shrink Small Outline Packages, Height is ≤ 1.60 mm, 0.50 mm Pitch | **TSSOP50P** + Lead Span Nominal - Pin Qty |
| Thin Shrink Small Outline Packages, Height is ≤ 1.60 mm, 0.40 mm Pitch | **TSSOP40P** + Lead Span Nominal - Pin Qty |
| Thin Shrink Small Outline Packages, Thin (Height is ≤ 1.60 mm) 0.30 mm Pitch | **TSSOP30P** + Lead Span Nominal - Pin Qty |
| Very Small Outline Packages, 0.762 mm Pitch (0.30 in Pitch) | **VSOP762P** + Lead Span Nominal - Pin Qty |
| SOD (Example: **SOD3705 = SOD123**) | **SOD** + Lead Span Nominal + Body Width |
| SON - Dual No Lead Packages 0.3 - 0.8 mm Pitch | **SON** + Pitch (**P**) - Body Width **X** Body Length - Pin Qty + Thermal Pad |
| SOT89 (JEDEC Standard Package) | **SOT89** |
| SOT143 (JEDEC Standard Package) | **SOT143** |
| SOT343 (JEDEC Standard Package) | **SOT343** |
| SOT143 Reverse (JEDEC Standard Package) | **SOT143R** |
| SOT343 Reverse (JEDEC Standard Package) | **SOT343R** |
| SOT223 (JEDEC Standard Package) (Example: SOT230P700-4N) | **SOT** + Pitch (**P**) + Lead Span Nominal - Pin Qty |
| SOT Generic Package 0.65 mm Pitch | **SOT65P** + Lead Span Nominal - Pin Qty |
| SOT Generic Package 0.95 mm Pitch | **SOT95P** + Lead Span Nominal - Pin Qty |
| TO (Generic DPAK) (Example: TO228P970-3N) | **TO** + Pitch (**P**) + Lead Span + Pin Qty |

**3.2 Design Producibility** As part of the planning cycle of a product's development, a concurrent engineering task group should be assembled to determine the criteria for each new design. During this planning phase, the product function and configuration is clearly defined and the assembly process options outlined. Product size, component types, projected volume and the level of manufacturing equipment available may affect process options.

Following the substrate development, the assembly will be evaluated for many of the fundamentals necessary to insure a successful SMT process. Specific areas addressed during the evaluation include:

a) Land pattern concepts

b) Component selection

c) Mounting substrate design

d) Assembly methods

e) Method of test

f) Phototool generation

g) Meeting minimum solder joint requirements

h) Stencil fixture requirements

i) Wave solder fixture requirements

j) Providing access for inspection

k) Providing access for rework and repair

**3.2.1 SMT Land Pattern** The use of process proven land patterns for the solder attachment of surface mount devices will provide a benchmark to evaluate solder joint quality. Land pattern geometry and spacing utilized for each component type must accommodate all physical variables including size, material, lead contact design and plating.

**3.2.2 Standard Component Selection** Whenever possible, SMT devices should be selected from standard configurations. The standard components will be available from multiple sources and will usually be compatible with assembly processes. For those devices developed to meet specific applications, standard packaging is often available. Select a package type that will be similar in materials and plating of standard device types when possible.

**3.2.3 Circuit Substrate Development** Design the circuit substrate to minimize excessive costs. High-density surface mount technology often pushes the leading edge of substrate technology. When estimating circuit density, allow for the greatest latitude in fabrication processes and tolerance variables. Before adopting extreme fine-line and utilizing small plated holes, understand the cost impact, yield, and long-term reliability of the product.

**3.2.4 Assembly Considerations** Manufacturing efficiency includes component placement. Within the constraints of circuit function, maintaining a consistent spacing between components and common orientation or direction of polarized devices can have an impact on all steps of the assembly process. In addition, when common orientation is maintained, machine programming is simplified and component verification, solder inspection and repair are simplified (See Figures 3-9 and 3-18).

**3.2.5 Provision for Automated Test** Testability of the assembled circuit substrate must be planned well in advance. If component level In-Circuit Test (ICT) is necessary, one test probe contact area is required for each common node or net. Ideally, all probe contact lands are on one side, typically the secondary side (double sided test fixtures are significantly more expensive). Functional testing may also employ the same test nodes used for in-circuit test but will include all connectors that interface to cables and other assemblies.

**3.2.6 Documentation for SMT** Documentation used to fabricate the circuit substrate and assemble the product must be accurate and easy to understand. Details, specifications and notes will guide both the assembly processing and control the quality level of a product. Unique materials or special assembly instructions, such as moisture sensitivity and handling, should be included on the face of the detail drawings or in the documentation package.

**3.3 Environmental Constraints**

**3.3.1 Moisture Sensitive Components** Plastic encapsulated IC packages may be susceptible to absorbing moisture. The component manufacturer usually provides specialized packaging for these, and furnish instructions for use or maintaining those parts in a controlled storage environment. IPC/JEDEC J-STD-033 provides proper handling and testing methods such as for moisture sensitivity.

**3.3.2 End-Use Environment Considerations** Compounds, materials and assembly processes should consider the products end-use environment. Table 3-16 provides information on the end-use environment characteristics for nine basic environments.

**Table 3-16 Product Categories and Worst-Case Use Environments for Surface Mounted Electronics (For Reference Only)**

| Product Category (Typical Application) | Temperature, °C / °F[1] | | Worst-Case Use Environment | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Storage | Operation | Tmin[2] °C / °F | Tmax[2] °C / °F | ΔT[3] °C / °F | $t_D$[4] hrs | Cycles/year | Typical years of Service | Approx. Accept. Failure Risk, % |
| Consumer | -40/85 | 0/55 | 0/32 | 60/140 | 35/63 | 12 | 365 | 1-3 | 1 |
| Computers and Peripherals | -40/85 | 0/55 | 0/32 | 60/140 | 20/36 | 2 | 1460 | 5 | 0.1 |
| Telecomm | -40/85 | -40/85 | -40/-40 | 85/185 | 35/63 | 12 | 365 | 7-20 | 0.01 |
| Commercial Aircraft | -40/85 | -40/85 | -55/-67 | 95/203 | 20/36 | 12 | 365 | 20 | 0.001 |
| Industrial and Automotive - Passenger Compartment | -55/150 | -40/85 | -55/-67 | 95/203 | 20/36<br>&40/72<br>&60/108<br>&80/144 | 12<br>12<br>12<br>12 | 185<br>100<br>60<br>20 | 10-15 | 0.1 |
| Military (ground and shipboard) | -40/85 | -40/85 | -55/-67 | 95/203 | 40/72<br>&60/108 | 12<br>12 | 100<br>265 | 10-20 | 0.1 |
| Space<br>leo<br>geo | -40/85 | -40/85 | -55/-67 | 95/203 | 3/5.4<br>to 100/180 | <br>1<br>12 | <br>8760<br>365 | 5-30 | 0.001 |
| Military Aircraft<br>a<br>b<br>c | -55/125 | -40/85 | -55/-67 | 125/257 | 40/72<br>60/108<br>80/144 | 2<br>2<br>2 | 100<br>100<br>65 | 10-20 | 0.01 |
| Maintenance | | | | | &20/36 | 1 | 120 | | |
| Automotive (under hood) | -55/150 | -40/125 | -55/-67 | 125/257 | 60/108<br>&100/180<br>&140/252 | 1<br>1<br>2 | 1000<br>300<br>40 | 10-15 | 0.1 |

& = in addition
1. All categories may be exposed to a process temperature range of 18°C to 260°C [64.4°F to 500°F].
2. Tmin and Tmax are the operational (test) minimum and maximum temperatures, respectively, and do not determine the maximum ΔT.
3. ΔT represents the maximum temperature swing, but does not include power dissipation effects; for power dissipation calculate ΔT; power dissipation can make pure temperature cycling accelerated testing significantly inaccurate. It should be noted that the temperature range, ΔT, is not the difference between Tmin and Tmax ; ΔT is typically significantly less.
4. The dwell time, $t_D$, is the time available for the creep of the solder joints during each temperature half-cycle.

See IPC-SM-785 and IPC-9701 for details regarding component and assembly testing.

**3.4 Design Rules** The printed board design principles recommended in this standard consider current test and manufacturing capabilities. Exceeding the limitation of these capabilities requires concurrence of all participants in the process including manufacturing, engineering and test technology. Involving test and manufacturing early in the design helps to move a quality product quickly into production.

Manufacturing engineering should be consulted regarding any components outside the scope of this document.

**3.4.1 Component Spacing**

**3.4.1.1 Component Considerations** The land pattern design and component spacing affect the reliability, manufacturability, testability and repairability of surface mount assemblies. A minimum inter-package spacing is required to satisfy all these manufacturing requirements. Maximum inter-package spacing is limited by several factors, such as available board space, equipment, weight considerations, and circuit operating speed requirements. Some designs require that surface mount components be positioned as close to one another as possible.

**3.4.1.2 Wave Solder Component Orientation** On any printed board assembly where surface mount devices are to be wave soldered, the orientation of devices in respect to the solder wave can contribute to excessive solder process defects. The preferred orientation compared in Figure 3-6 optimises the solder process, minimizing solder bridging on the trailing or shadowed contacts as the assembly exits the solder wave. All polarized surface mount components should be placed in the same orientation when possible. The following additional conditions apply:

a) All passive components should be parallel to each other.

b) The longer axis of SOICs and the longer axis of passive components shall be perpendicular to each other.

c) The long axis of passive components shall be perpendicular to the direction of travel of the board along the conveyer of the wave solder machine.

**3.4.1.3 Component Placement** Similar types of components should be aligned on the board in the same orientation for ease of component placement, inspection, and soldering. Also, similar component types should be grouped together whenever possible, with the net list or connectivity and circuit performance requirements ultimately driving the placements. In memory boards, for example, all of the memory chips are placed in a clearly defined matrix with pin one orientation in the same direction for all components. This is a good design practice to carry out on logic designs where there are many similar component types with different logic functions in each package. On the other hand, analogue designs often require a large variety of component types making it understandably difficult to group similar components together. Regardless of whether the design is memory, general logic, or analog, it is recommended (when possible) that the orientation of pin 1 on all IC components is the same, provided that product performance or function is not compromised.

**3.4.1.4 Grid-Based Component Positioning** SMT component placement is generally more complex than PIH printed boards for two reasons: higher component densities, and the ability to put components on both sides of the board. In high-density SMT designs the spacing between lands of different components are often less than 0.2 mm. Grid-based SMT device placement may not be practical due to the large variety of component shapes.

Two effects created by random component placement are a loss of uniform grid-based test node accessibility and a loss of logical, predictable routing channels on all layers (possibly driving layer counts). In addition, the accepted international grid identified in IPC-1902 states that for new designs the grid should be 0.5 mm, with a further subdivision being 0.05 mm. One solution to the problem is to build CAD libraries with all component lands connected to vias on 0.5 mm centers (or greater, based on design) to be used for testing, routing, and rework ports.

It is easier to process a printed board (PB) that has uniform component center-point spacing cross the board in both directions (see Figure 3-7).

**3.4.2 Single- and Double-Sided Board Assembly** The term single-sided board assembly refers to components mounted on one side, and the term double-sided refers to components mounted on both sides of the board. The double-sided board assembly may require additional solder and assembly process steps and can increase manufacturing cost. Designers should concentrate on locating all components on the primary side of the board whenever possible.

**3.4.2.1 Solder Paste Stencil** The solder stencil is the primary vehicle by which solder paste is applied to the

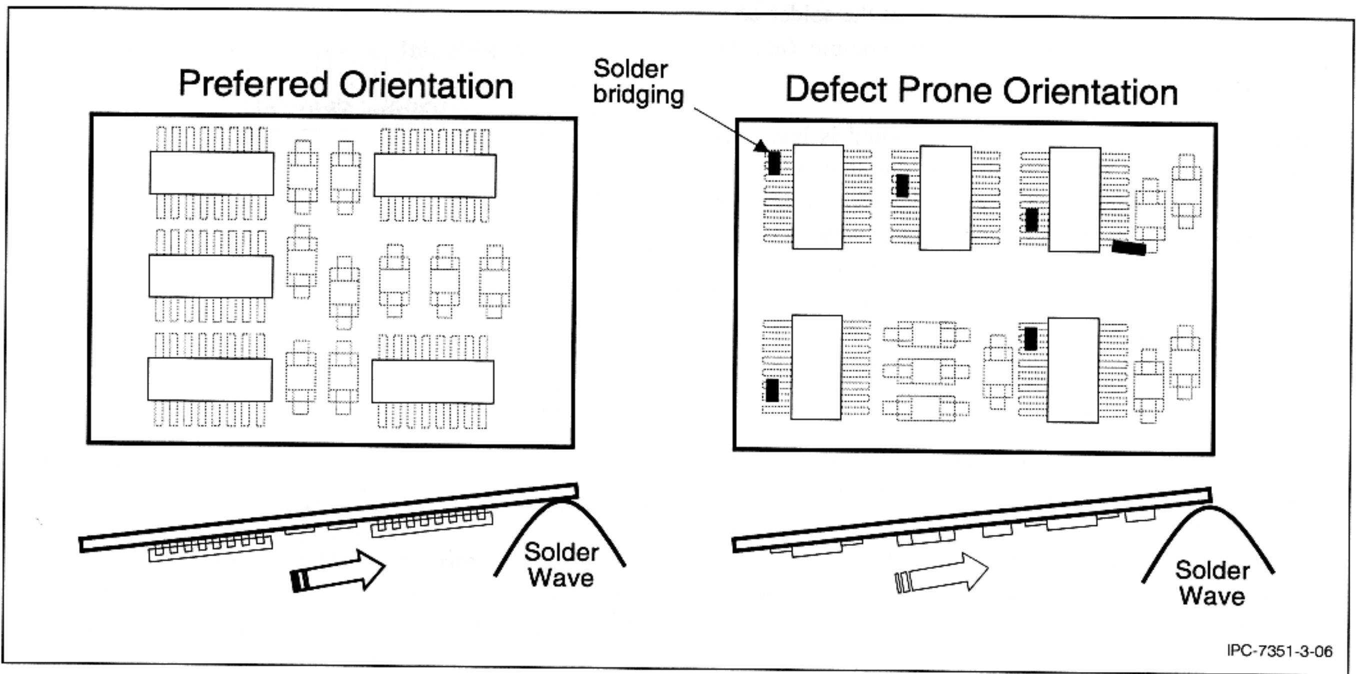



**Figure 3-6 Component Orientation for Wave-Solder Applications**

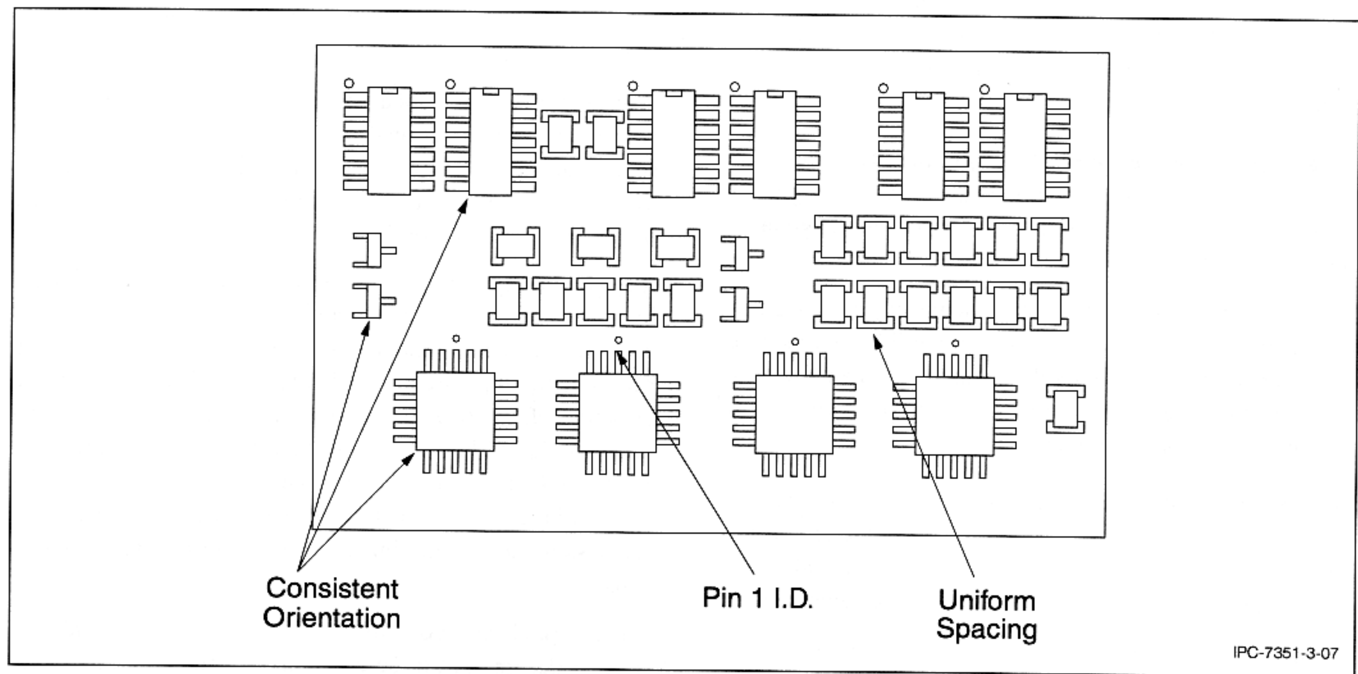



**Figure 3-7 Alignment of Similar Components**

SMT printed board. With it, the exact location and volume of solder paste deposition is precisely controlled. The artwork for developing the stencil is the component mounting lands from the outer layers of the board with all other circuitry deleted. The information provided for the openings in the stencil is usually indicated as being the same size as the lands on the board for all components. This information (or data) may be selectively modified by the printed board assembler or process engineer who will define the specific adjustments required to meet specific solder volume requirements (see IPC 7525).

The optimum stencil thickness is determined by evaluating the solder paste requirements for all the components to be reflow soldered. This should be based on study of the minimum and target requirements for SMT solder joints given in IPC/EIA-J-STD-001.

Ideally, the volume deposited should be the total amount required to achieve the "target" solder joint condition (see IPC-A-610), less the solder already available on the land and termination or lead (the latter can together amount to 10% to 20% of the total and should not be ignored). In

making calculations, it should be noted that the solder content of most pastes is 50% to 55% by volume (not by weight), depending on particle size.

If the amount of solder paste to be deposited is less than the amount provided by using an aperture at or near the land area size, a reduced area of print should be placed in the best position on the land to assure good wetting of the joint areas. In some cases, this may best be achieved by reducing the width of the print, in others, the length. For very fine pitch with inter-land gaps of less than 0.2 mm, staggering (offsetting) the print at alternate ends of the lands can reduce the risk of shorts after soldering.

If the amount of solder paste required is more than the amount available using the geometry provided for the basic land pattern on the PCB the aperture size in the stencil can be enlarged to increase solder volume. The amount and direction of the overhang of the printed solder beyond the land is dictated by the space available around the land and the need to avoid shorting and solder bridging if excess overhang occurs. The tolerances on land position and printing accuracy need to be considered when calculating the maximum allowable over-print. See IPC-7525 for the design and fabrication of stencils for surface mount solder paste application.

**3.4.3 Component Stand-off Height for Cleaning** The recommended minimum component stand-off height for cleaning is affected by the distance across the diagonal of the component lead pitch.

If a minimum stand-off cannot be achieved, proper cleaning under the component may not be possible. In this case, it is recommended that a no-clean flux be used and/or mask material should be retained over all exposed via and circuit patterns located under devices.

**3.4.4 Fiducial Marks** A fiducial mark is a printed artwork feature created in the same process as the circuit artwork for optical recognition systems. The fiducial and a circuit pattern artwork must be etched in the same step.

The fiducial marks provide common datum points for all steps in the assembly process. This allows each piece of equipment used for assembly to accurately locate the circuit pattern. There are two types of fiducial marks.

**3.4.4.1 Panel and Global Fiducials** Global fiducial marks are used to locate the position of all circuit features on an individual board. When a multi-image circuit is processed in panel form, the global fiducials are referred to as panel fiducials (see Figure 3-8).

A minimum of two global fiducial marks is required for correction of offsets (x and y position) and rotational offsets (theta position). These should be located diagonally opposite and as far apart as possible on the circuit or panel.

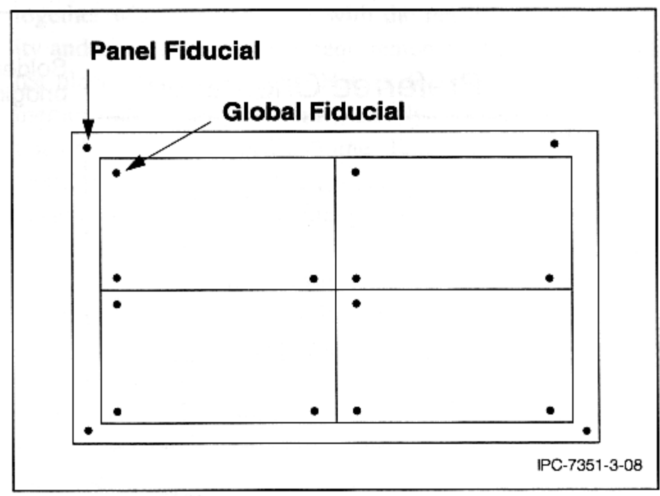



**Figure 3-8 Panel/Local Fiducials**

A minimum of three fiducial marks is required for correction of nonlinear distortions (scaling, stretch and twist). These should be located in a triangular position as far apart as possible on the circuit or panel.

**3.4.4.2 Local Fiducials** Local fiducial marks are used to locate the position of an individual component requiring more precise placement.

A minimum of two local fiducial marks are required for correction of translational offsets (x and y position) and rotational offsets (theta position). This can be two marks located diagonally opposed within or outside the perimeter of the land pattern (see Figure 3-9).

It is good design practice to locate global or panel fiducials in a three-point grid-based datum system as shown in Figure 3-10. The first fiducial is located at the 0-0 location. The second and third fiducials are located in the X and Y directions from 0-0 in the positive quadrant. The global fiducials should be located on the top and bottom layers of all printed boards that contain surface mount as well as through-hole components since even through-hole assembly systems are beginning to utilize vision alignment systems.

All fine pitch components should have two local fiducial systems designed into the component land pattern to insure that enough fiducials are available every time the component is placed, removed and/or replaced on the board. All fiducials should have a soldermask opening large enough to keep the optical target absolutely free of soldermask. If soldermask should get onto the optical target, some vision alignment systems may be compromised due to insufficient contrast at the target site.

If space is limited, one may be able to share a fiducial from an adjacent component within the location constraint (see Figure 3-10).

**3.4.4.3 Size and Shape of Fiducial** The optimum fiducial mark is a solid filled circle. The preferred diameter of

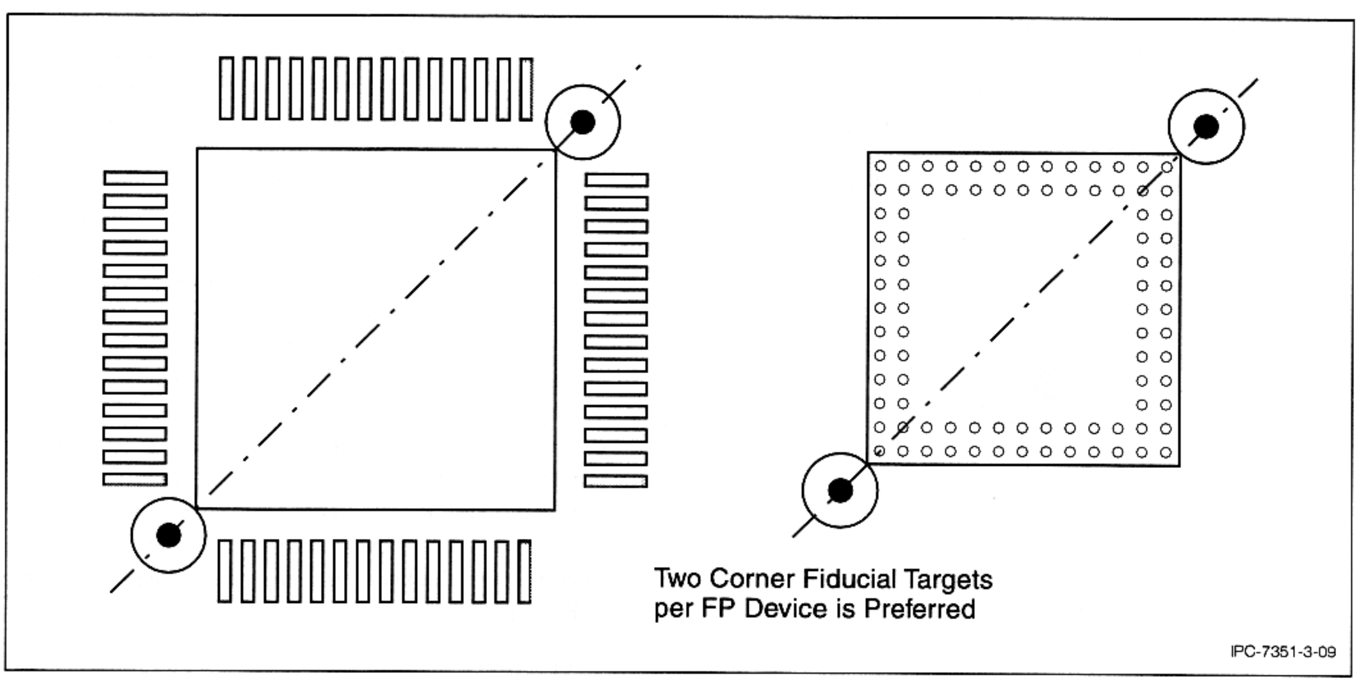



Figure 3-9 Local Fiducials

Local fiducial targets for Fine Pitch ICs

F2

Sharing of fiducials
among adjacent
components

F1

F3

Global fiducial targets

IPC-7351-3-10

Figure 3-10 Fiducial Locations on a Printed Board

the fiducial mark is 1.0 mm. The maximum diameter of the mark is 3.0 mm. Fiducial marks should not vary in size on the same PCB more than 25 µm. A clear area devoid of any other circuit features or markings shall exist around the fiducial mark. The minimum size of the clear area shall be equal to twice the radius of the mark (see Figure 3-11).

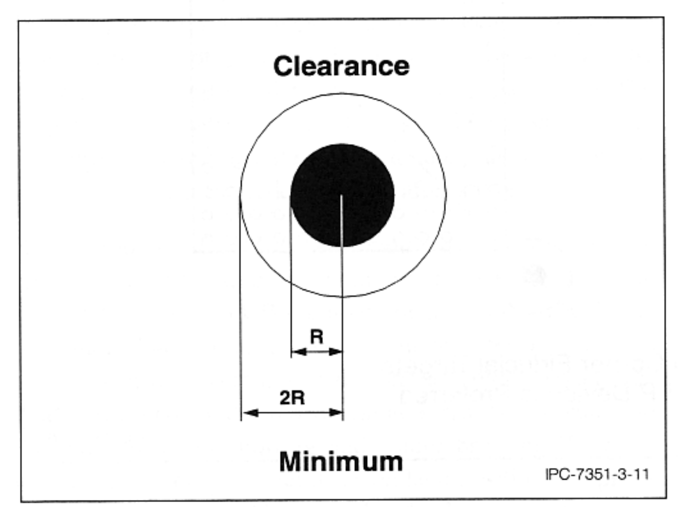



**Figure 3-11 Fiducial Size and Clearance Requirements**

**3.4.4.4 Zonal Fiducials** To ensure the accurate placement of multiple surface mount components that are not near 'component specific local fiducials' or 'global fiducials', additional 'zonal fiducial targets' may be placed within a zone or an area of the board assembly to compensate for board dimensional stability.

**3.4.4.5 Material** The fiducial mark may be bare copper, bare copper protected by organic coating or metal plating. If solder mask is used, it should not cover the fiducial mark or the clearance area. It should be noted that excessive oxidation of a fiducial mark's surface may degrade its readability.

**3.4.4.6 Flatness** The flatness of the surface of the fiducial mark should be within 15 µm.

**3.4.4.7 Edge Clearance** The edge of the fiducial should be no closer to the board edge than the sum of 4.75 mm and the minimum fiducial clearance required. If less than this sum, a board handling fixture may be required.

**3.4.4.8 Contrast** Best performance is achieved when a consistent high contrast is present between the fiducial mark and the PCB base material.

The background for all fiducial marks must be the same. That is, if solid copper planes are retained under fiducials in the layer below the surface layer, all fiducials must retain uniform background. If copper is clear under one fiducial, all must be clear.

### 3.4.5 Conductors

**3.4.5.1 Conductor Width and Spacing** Increased component density on SMT designs has mandated the use of thinner copper, narrower conductor width and spacing. Higher component density may increase PCB layer counts as well, requiring the use of more vias to make the necessary connections between layers (see Figure 3-12).

**3.4.5.2 Inner Layer Conductors** The use of wider conductors and spacing often drives layer counts up because there is less routing channel available between vias. It is for this reason that there is an increased usage of narrower conductors on internal layers. Figure 3-13 compares the number of routing channels available between lands using the 0.15 mm geometry. Since conductor width control is much more difficult to maintain on outer layers of the PCB, it is better to keep the narrower conductor geometries on the inner layers of a multilayer printed board. Generally, the option of using narrow geometries is driven by the need to reduce layer counts. Decreasing layer counts may reduce the overall board thickness and improve the aspect ratio for small hole drilling.

### 3.4.6 Via Guidelines

**3.4.6.1 Drilled Via Holes** The size of the via holes should be selected on the basis of the printed board thickness versus the hole diameter or aspect ratio limits as defined by the printed board fabricator. In addition, specific via lands and holes can be accessed for automatic in-circuit test (ICT). Figure 3-14 shows the land-pattern-to-via relationships.

**3.4.6.2 Vias and Land Pattern Separation** For reflow soldering, via lands must be located away from the component lands to prevent solder migration. This migration will cause insufficient solder fillets on components. The solder migration can be restricted by providing a narrow conductor between the land area and the via or prevented by using the soldermask over bare copper circuitry. The relationship for mounting land and via locations should consider the conductor routing requirements. Figure 3-15 provides several examples of via positioning concepts.

Wide conductors connecting to a land area can act as a solder thief by drawing solder away from the land and down the conductor. Furthermore, if the conductor goes to a via which is connected to an inner layer power or ground plane, the plane may act as a heat sink and draw heat away from the land/lead area during reflow solder resulting in a defective solder joint.

Specifying soldermask tented or filled vias will prevent solder migration on assemblies manufactured with a solder reflow process. Filled or tented vias also take care of potential flux entrapment problems under components and are highly desirable for attaining good vacuum seal during in-circuit bed-of-nails testing. Tenting is typically done with a dry film type of soldermask, or if via holes are very small, may be plugged and tented using liquid soldermask.

Surface Mount
Componant Land Pattern

Plated via for interface
between the outer circuit
layer and subsurface layer
or layers of the board.

External Surface
Routed Circuits

Internal Connection

Internal Subsurface
Route Circuit Layer

IPC-7351-3-12

**Figure 3-12 Use of Vias in High Component Density Printed Circuit Boards**

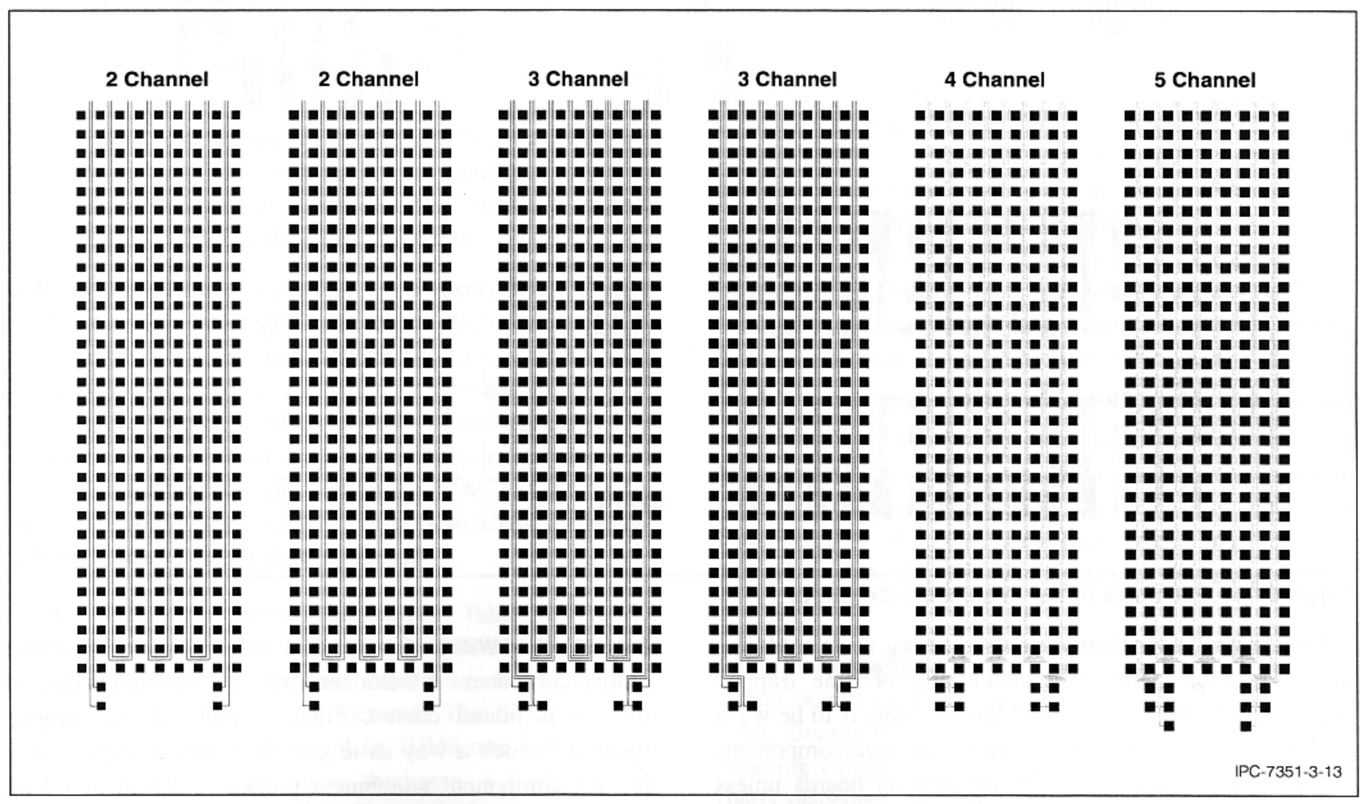



**Figure 3-13 Conductor Routing Capability Test Pattern**

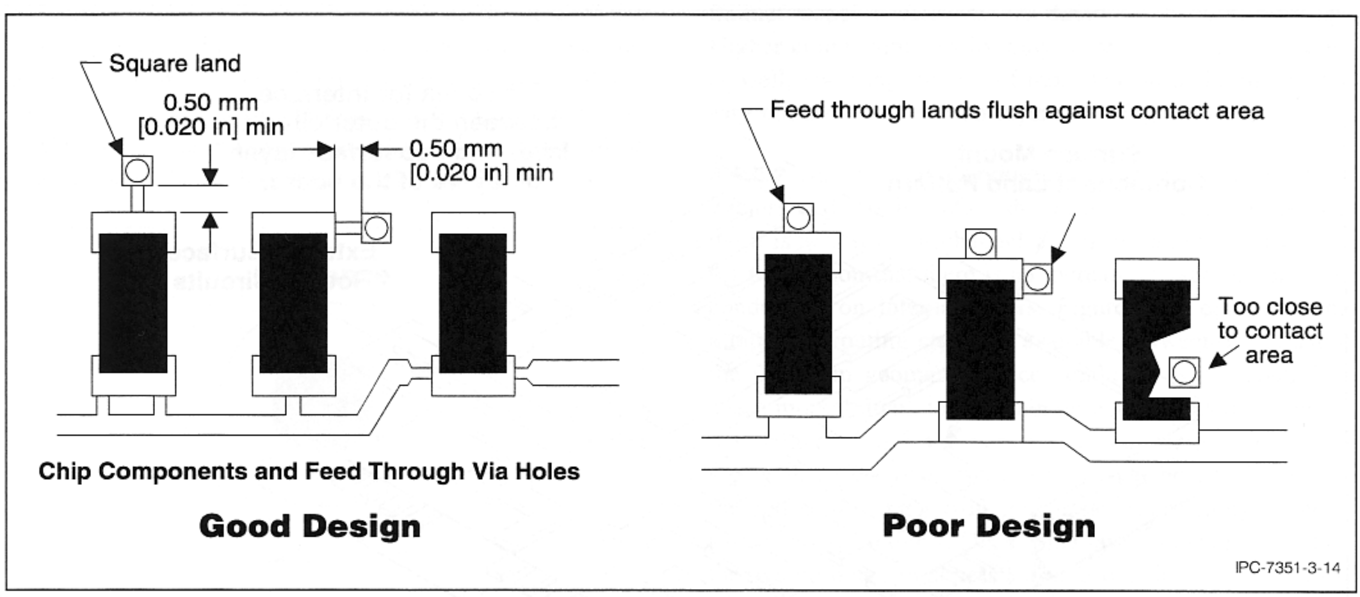



**Figure 3-14 Land Pattern to Via Relationship**

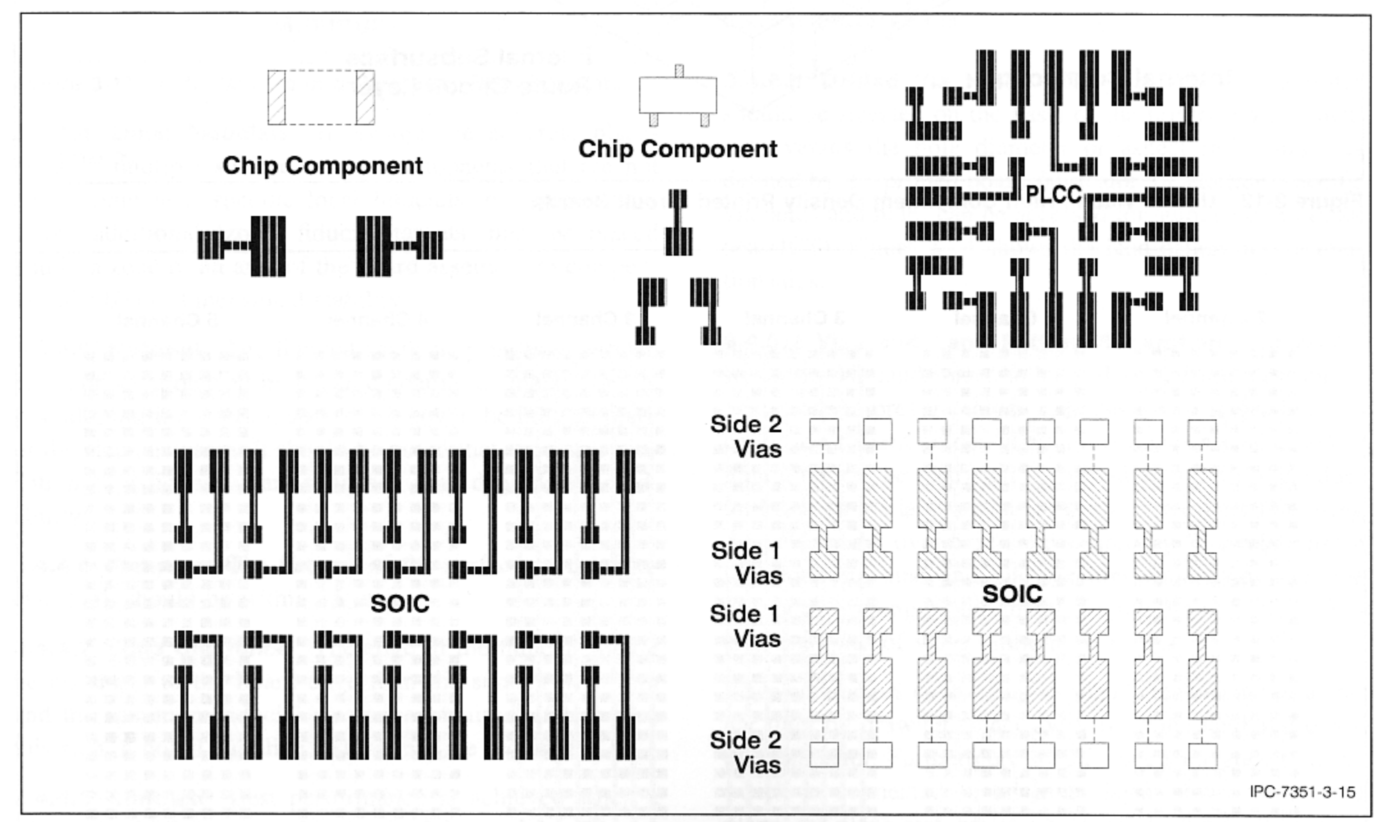



**Figure 3-15 Examples of Via Positioning Concepts**

**3.4.6.3 Vias Under Components** During wave soldering of the assembly, flux may potentially become trapped under zero clearance devices. If the assembly is to be wave soldered, via holes underneath zero clearance components on the primary side should be avoided on boards unless vias are tented with soldermask. Untented via holes may be located underneath zero clearance surface mount packages in reflow soldered surface mount assemblies that will not be exposed to wave soldering (see Figure 3-16).

**3.4.6.4 Vias Within Lands** Via holes within the surface mount component attachment lands are permitted only if the via is plated closed, filled or plugged and capped (plated) in such a way as to prevent solder migration during the component attachment process. A blind or plated closed micro-via in the land is typically acceptable for solder attachment of surface mount components. Refer to IPC-2226 for minimum annular ring requirements for microvias.

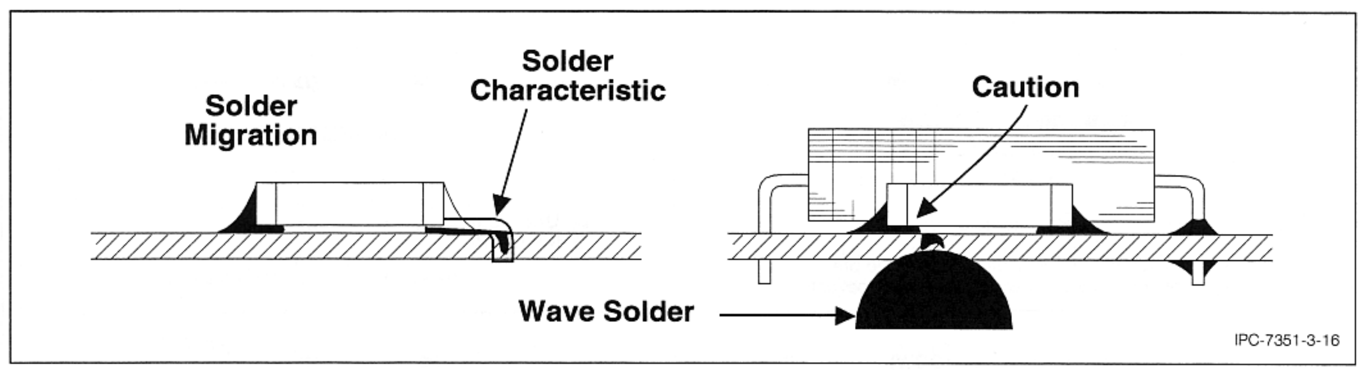



**Figure 3-16 Vias Under Components**

**3.4.6.5 Vias as Test Points** Via holes, in addition to being used for connecting surface mounted component lands to conductor layers, may also be used as test targets for bed-of-nails type probes and/or rework ports. When a via is used as a test point it is required that the x-y location and size of a test land be defined as a secondary file for test fixture development.

**3.4.7 Standard PCB Fabrication Allowances** Manufacturing tolerances or standard fabrication allowances (SFA) exist in all PCB fabrication shops. Virtually every registration or alignment operation that is performed has some potential for misregistration. There are approximately 42 basic steps in fabricating a multilayer PCB, several of which involve operations that require precision in location and alignment. The tolerance varies according to the printed board maximum diagonal dimension and must be included in the land size calculations. The fabricator should be consulted prior to beginning a design to determine their SFA. With this SFA value, the designer can proceed accordingly, preventing tolerances from stacking up and creating yield and/or production problems.

**3.4.7.1 PCB Manufacturing Characteristics** Figure 3-17 shows the various characteristics of conductor geometry after etching. End-product drawings and specifications should specify only the minimum for conductor spacing; however, conductor widths should be defined according to minimum values, where land patterns should be defined as to their maximum material conditions (MMC). Clear target values for conductors and land patterns will help the manufacturer achieve the desired condition.

**3.4.7.2 Conductor Width Tolerances** Table 3-17 represents process tolerances that can be expected with normal processing. (Specific process tolerances should be discussed with the board manufacturer.) The bilateral tolerances in Table 3-17 are typical for 0.046 mm [0.00181 in] copper. For additional copper thickness, a further width variation can be expected (see Figure 3-17).

**3.4.7.3 Conductive Pattern Feature Location Tolerance** Table 3-18 is for the tolerance to be applied to the nominal dimension chosen for the location of the lands, connector contacts and conductors in relation to the datum reference. These tolerances include master pattern accuracy, material movement, layer registration and fixturing.

**3.4.7.4 Annular Ring Control** Annular ring is defined as the amount of land that remains after a hole is drilled through it. With high-density SMT designs, maintaining minimum annular requirements has emerged as one of the most difficult parts of multilayer PCB fabrication in terms of producibility. Perfect registration will maximize the annular ring all around the drilled hole.

For example, using a 0.8 mm [0.0315 in] land with a 0.5 mm [0.0197 in] drill will result in a 0.15 mm [0.00591 in] annular ring under perfect registration conditions. If misregistration of 0.15 mm [0.00591 in] occurs in any direction, the result will be a 0.3 mm [0.012 in] annular ring on one side of the pad, and no annular ring on the other side. If misregistration is greater than 0.15 mm [0.00591 in], i.e., 0.2 mm [0.0079 in], then the drill will actually break out of the land. If the breakout is in the direction where the conductor connects to the land, the drill will effectively disconnect the conductor from the land. The net result is a scrapped PCB. Since signal conductors intersect the lands from all directions, any breakout has the potential to randomly disconnect conductors all over the PCB.

Maintaining consistent annular ring control is difficult, but methods have been developed to insure connectivity between lands and conductors. Each method is intended to provide copper material where the conductor enters the land. The land which has the added material may resemble a teardrop or keyhole or adopt alternate designs as shown in Figure 3-18.

**3.4.8 Panelization** Components can be mounted on individual boards or on boards that are organized in a panel form. Boards or panels that will be moved by automatic handling equipment or pass through automated operations (parts placement, soldering, cleaning, etc.) must have specific areas kept free of parts or active circuitry. Typically, a clear area of 3.0 mm [0.012 in] to 5.0 mm [0.0197 in] wide must be allowed along the sides for the clearance. The required clearance width is dependent upon the design of

Resist
V
X
Laminate
Etch Factor = $\frac{V}{X}$
An etch factor of 1/1 is usually considered practical.
Higher factors may be specified for some applications.

"B" (DCW)
"C" Undercut & Overhang
"A" (MCW)*
**Panel Plating** (Dry Film Resist)

"B" (DCW)
"E" Outgrowth
"C" Undercut
Overhang
"A" (MCW)*
**Panel Plating** (Liquid Resist)

(OCW)*
"D"
"B" (DCW)*
"C" Undercut
"E" Outgrowth
Overhang
"A" (MCW)*
**Pattern Plating** (Dry Film Resist)

(OCW)*
"D"
"E" Outgrowth
"B" (DCW)*
(MCW)*
"A"
**Pattern Plating** (Liquid Resist)

"B" (DCW)*
"C" Undercut
**Thin Clad & Pattern Plating** (Dry Film Resist)

**A = MCW** (Minimum Conductor Width) **B = DCW** (Design Conductor Width) **D = OCW** (Overall Conductor Width)

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**Figure 3-17 Conductor Description**

**Table 3-17 Conductor Width Tolerances, 0.046 mm [0.00181 in] Copper, mm [in]**

| Feature | Producibility Level A | Producibility Level B | Producibility Level C |
|---|---|---|---|
| Without plating | ± 0.06 mm [± 0.00236 in] | ± 0.04 mm [± 0.00157 in] | ± 0.015 mm [± 0.0005906 in] |
| With plating | ± 0.10 mm [± 0.00393 in] | ± 0.08 mm [± 0.00314 in] | ± 0.05 mm [± 0.0197 in] |

**Table 3-18 Feature Location Accuracy (units: mm [in])**

| Greatest Board/ X,Y Dimension | Producibility Level A | Producibility Level B | Producibility Level C |
|---|---|---|---|
| Up to 300 [11.81] | 0.30 [0.012] | 0.20 [0.00787] | 0.10 [0.00394] |
| Up to 450 [17.72] | 0.35 [0.0138] | 0.25 [0.00984] | 0.15 [0.00591] |
| Up to 600 [23.62] | 0.40 [0.0157] | 0.30 [0.012] | 0.20 [0.00787] |

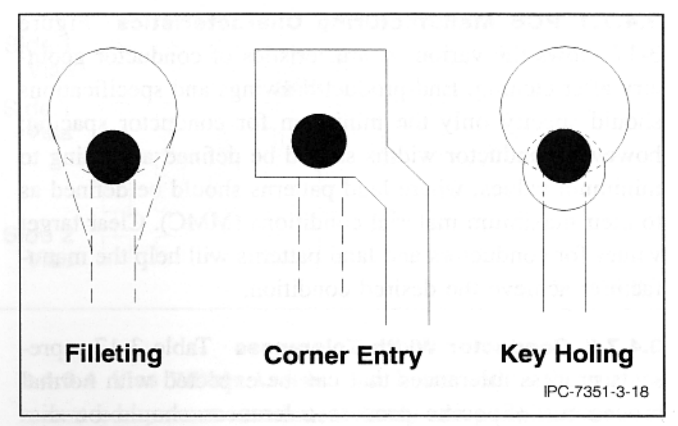



**Figure 3-18 Examples of Modified Landscapes**

the board handling and fixturing equipment. These dimensions should be obtained from the process equipment manufacturer before board or panel design (see Figure 3-19).

Special tooling and fixturing holes are generally located within the edge clearance areas. The clearance areas are needed to avoid interference with board handling fixtures, guidance rails and alignment tools.

For accurate fixturing, two or more nonplated holes are located in the corners of the board to provide accurate mechanical registration on board transfer equipment. Board handling holes (typically 3.2 mm [0.126 in]) may also be located in the clearance areas. These holes may be used by automated board handling equipment or for test fixture alignment. Specific panel size should be obtained from the equipment manufacturer or process engineer.

**3.4.8.1 Board Size and Panel Construction** In order to fully utilize the automation technology associated with surface mount components, a designer should consider how a printed board or P&I structure will be fabricated, assembled and tested. Each of these processes, because of the particular equipment used, may require fixturing, which will affect or dictate certain facets of the board layout. Tooling holes, panel size, component orientation and clearance areas (both component and conductor) on the primary and secondary sides of the board are all equipment and process dependent.

To produce a cost-effective layout through optimum base material utilization, a designer should consult with the board manufacturer to determine optimum panel size. The board should be designed to utilize the manufacturer's suggested usable area. Smaller boards can be ganged or nested in a uniform panel format to simplify fixturing and reduce excessive handling during assembly. Panel layout is typically defined by an assembly process specialist or the manufacturing service provider.

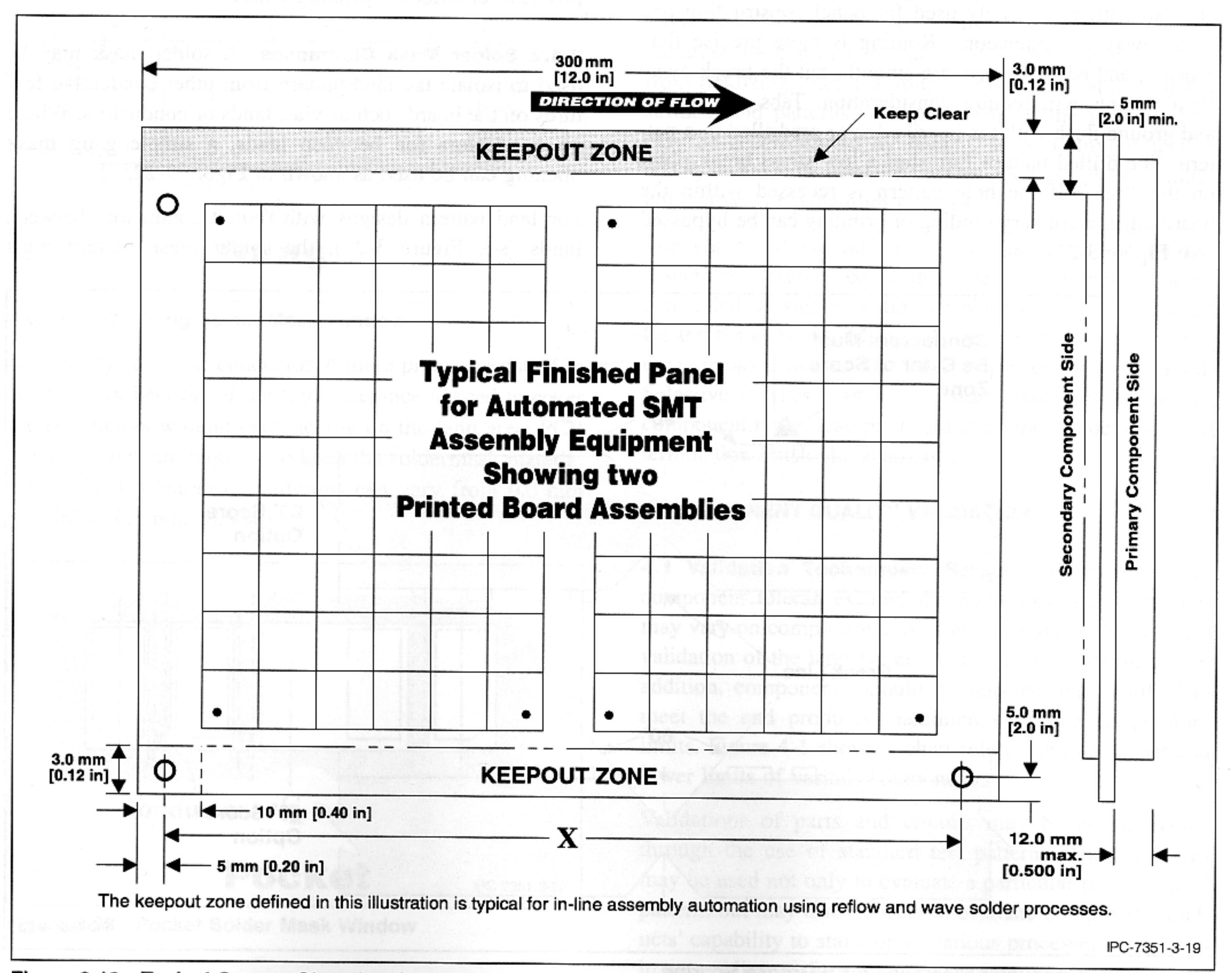



**Figure 3-19 Typical Copper Glass Laminate Panel**

Panel construction may include several boards arranged in a matrix or simply one board requiring additional material retained for efficient assembly processing. The large board or several smaller boards are retained in the panels and separated after all assembly processes are completed. Excising or separating the individual boards from the panel must be planned as well. Several methods are used to retain circuits in a panel, including V-groove scoring, NC routing and routed slot with break-away tabs.

**3.4.8.2 V-Groove Scoring** V-groove scoring may be provided to enable post assembly separation. The groove feature is generally provided on both surfaces of the board and only in a straight line. A small cross-section of board material is retained at the break line. An allowance for the scoring angle must be made as well. Conductors that are located too close to the score groove will be exposed or damaged, and rough edges must be sanded lightly to remove burrs and rough fabric particles (see Figure 3-20).

**3.4.8.3 Routed Slot and Tab Features** The routed slot and tab pattern is widely used for panel construction and break-away tab extensions. Routing is more precise than scoring, and edge surfaces are smooth, but the break-away "tab" points will require consideration. Tabs can be cut and ground flush with the board edge or predrilled in a pattern. The drilled pattern furnishes a low stress break point on the "tab." If the hole pattern is recessed within the board edge, secondary sanding or grinding can be bypassed (see Figure 3-21).

## 3.5 Outer Layer Surface Finishes

**3.5.1 Solder Mask Finishes** Solder mask coatings are used to protect the circuitry on the printed board. Solder mask coatings are available in two forms, liquid and dry film. The polymer mask material is applied using several process methods and is furnished in varying thicknesses. As an example, liquid materials will have a finished thickness of 0.02 mm [0.0079 in] to 0.025 mm [0.00984 in] while the dry film products are supplied in thicknesses of 0.04 mm [0.016 in], 0.08 mm [0.0315 in], and 0.10 mm [0.0394 in]. Although screen type printing for solder mask is available, photo-imaged soldermask is recommended for surface mount applications.

The photo process provides a precise pattern image and when properly developed eliminates mask residue from land pattern surfaces. The mask thickness may not be a factor on most surface mount assemblies but, when fine pitch (0.63 mm [0.0248 in] or less) IC devices are mounted on the printed boards, the lower profile soldermask will provide better solder printing control.

**3.5.2 Solder Mask Clearances** A solder mask may be used to isolate the land pattern from other conductive features on the board such as vias, lands or conductors. Where no conductors run between lands, a simple gang mask opening can be used as shown in Figure 3-22.

For land pattern designs with routed conductors between lands (see Figure 3-23), the solder mask pattern must

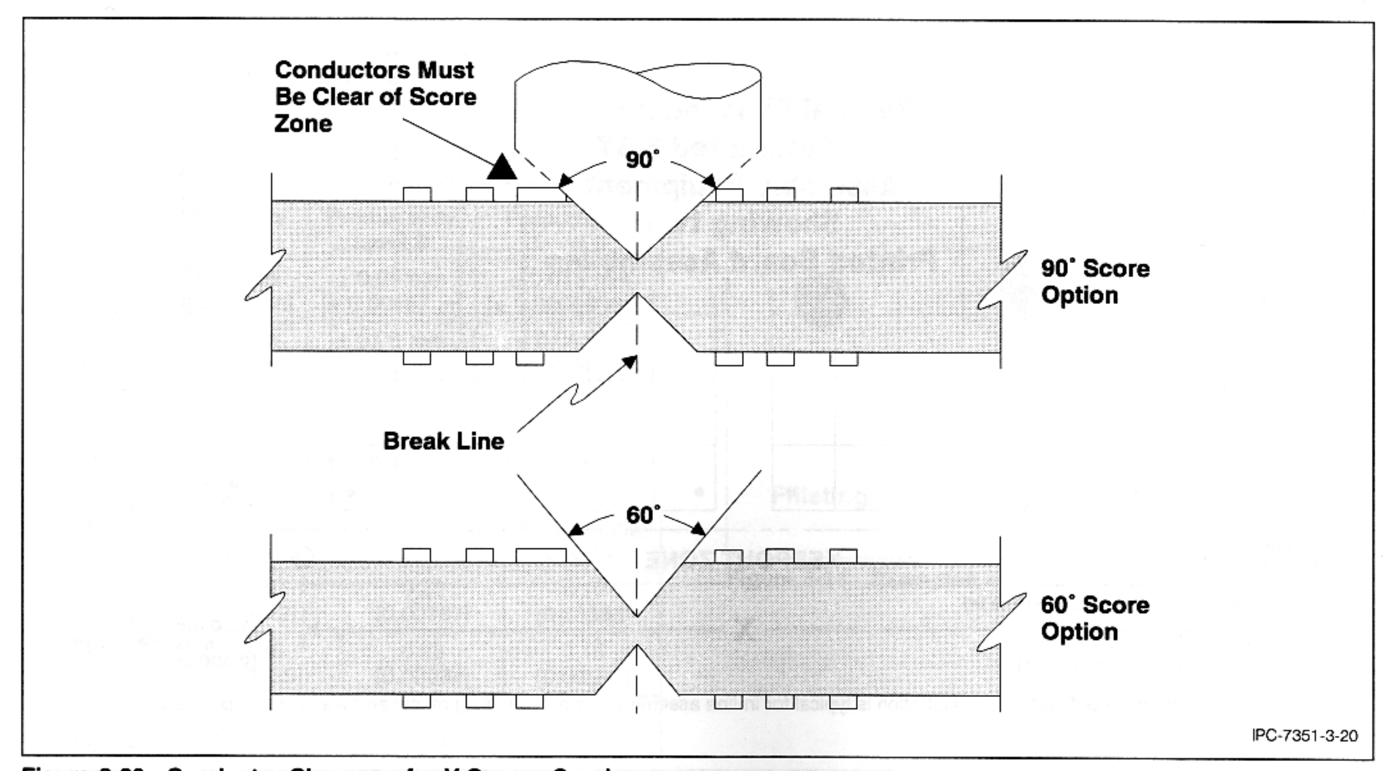



Figure 3-20 Conductor Clearance for V-Groove Scoring

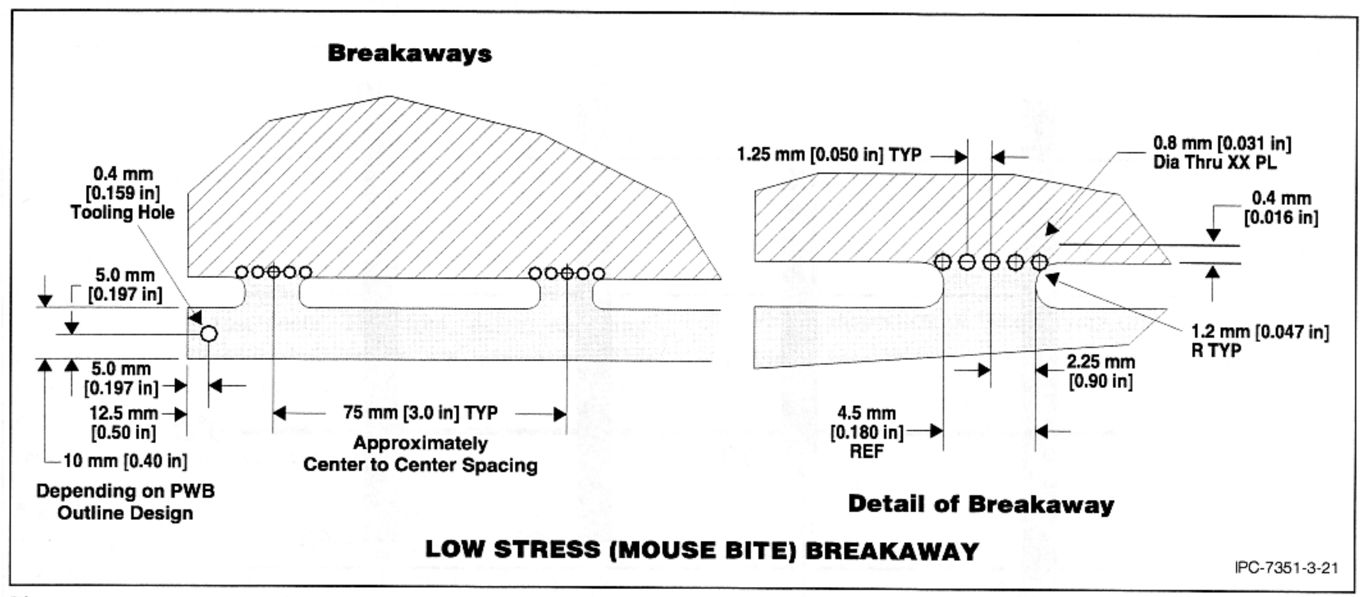



**Figure 3-21 Breakaway (Routed Pattern) with Routed Slots**

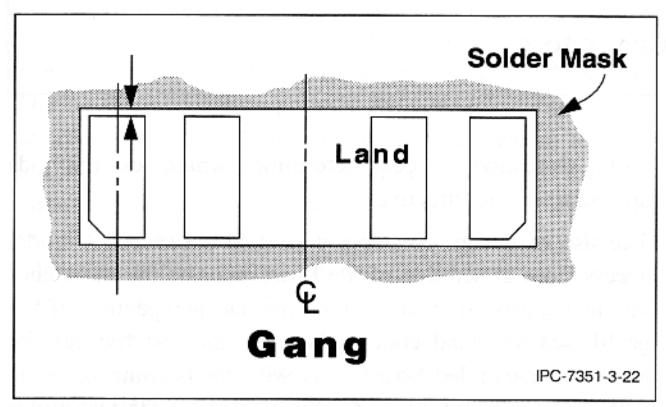



**Figure 3-22 Gang Solder Mask Window**

completely cover the conductor. A more precise registration is necessary because of the tight tolerance needed to cover the conductors without encroaching on the land area. PCB manufacturers are required to keep the soldermask material off the land. Clearance conditions can vary from 0.0 mm [0.0 in] to 0.1 mm [0.0040 in].

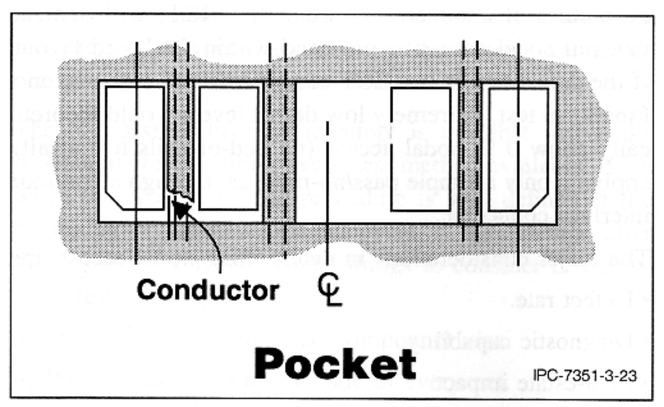



**Figure 3-23 Pocket Solder Mask Window**

**3.5.3 Land Pattern Surface Finishes** The soldermask openings expose the land patterns for attachment of surface mount components. These are usually copper-based and therefore need protection in order to prevent the copper from oxidizing, thus resulting in poor solderability of the surface land patterns. The protection of the land patterns may be accomplished by organic solderability protective (OSP) coatings or metallic finishes such as solder coating, gold, silver, or palladium platings.

The choice of coatings or plating is dependent on the assembler's preference or the type of components being assembled. A single coating or plating finish is preferred for the entire board. Mixing the surface finish types is not recommended due to the different process steps required. Selective finishes may be necessary based on the mix of component types, lead pitch and attachment process or lead termination finish characteristics.

## 4 COMPONENT QUALITY VALIDATION

**4.1 Validation Techniques** Because of the variety of component tolerances, and the possibility that tolerances may vary on components, users are encouraged to establish validation of the land pattern and component geometry. In addition, components should be selected and qualified to meet the end products maximum operating temperature limits. Figure 4-1 shows a chart referencing the upper and lower limits of various components.

Validations of parts and circuits may be accomplished through the use of standard test patterns. These patterns may be used not only to evaluate a particular part to a land pattern, but may also be used to evaluate component products' capability to stand up to various processes being used in assembling surface mounted parts.

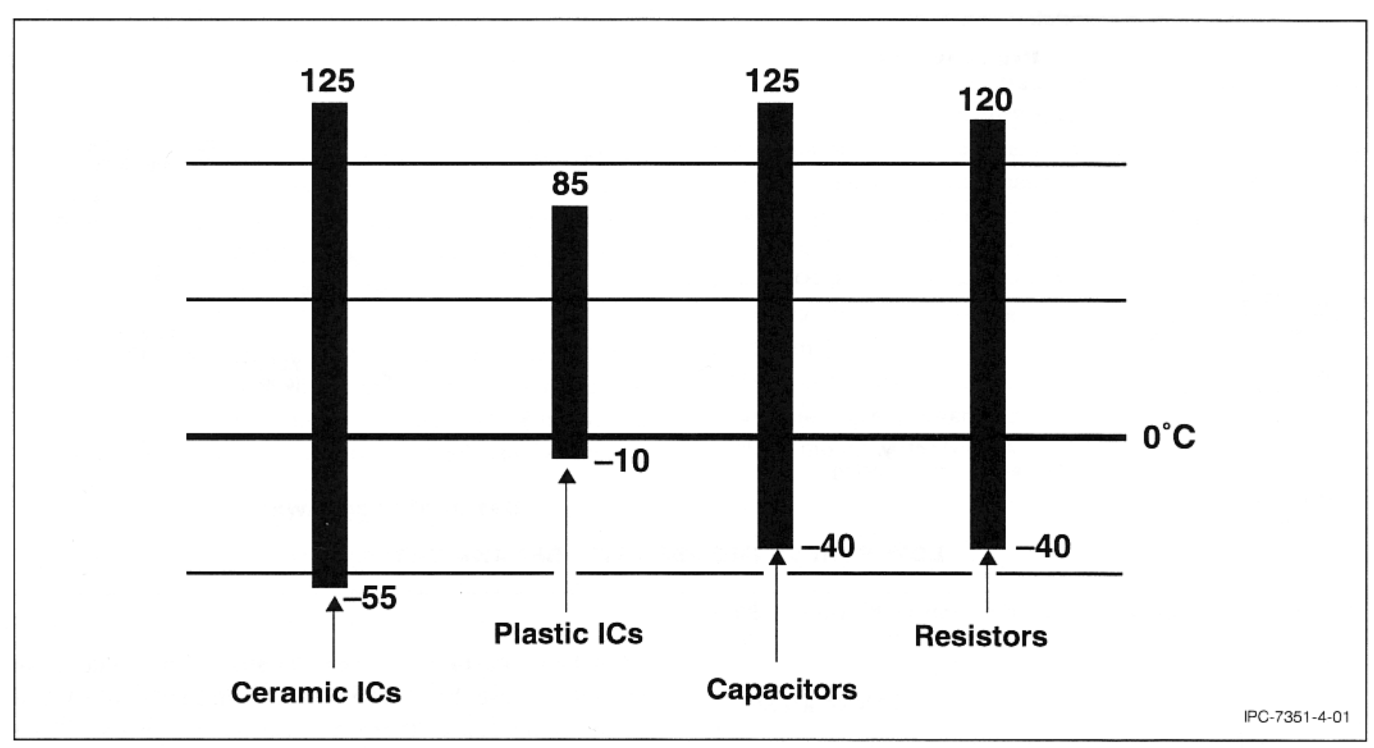



**Figure 4-1 Component Operating Temperature Limits**

## 5 TESTABILITY

**5.1 Board and Assembly Test** There are five basic types of tests which can be performed on SMT boards. These are:

a) Bare-board test which checks the unpopulated board for shorts and opens

b) Manufacturing defect analysis which checks the populated board for soldering shorts

c) In-circuit test operational verification of each individual component

d) Functional test operational verification of functional block of circuits

e) Combinational test limited integration of in-circuit and functional test

The first test type is a bare-board test performed by the board fabricator. The remaining four test types are loaded on assembled board tests and performed after assembly. The bare-board test should be mandatory, while the loaded board may be tested using any one or a combination of the four loaded board tests.

**5.1.1 Bare-Board Test** In testing printed boards using through-hole technology, the defect rate and the test methods chosen are the principle determiners of overall test cost. Real-estate considerations (specifically the percentage of nodes that are available for bed-of-nails probing) are not a concern, since the holes provide 100% nodal access. In testing surface mount boards, however, real-estate considerations (in addition to defect rates) have an impact on test costs, since nodal access determines which test methods are possible and effective.

The use of design concepts with grid-based 100% nodal access from either side of the board may be the most economical approach from the total process perspective. If the grid-based test land concept is used, the test fixtures for bare and assembled board tests will not become obsolete through later board connectivity revisions if the test nodes are not moved. Also, if the printed board uses buried vias, the grid-based test land concept with 100% nodal access may provide access to buried nets from the ends of the nets; this is a benefit realized during the bare-board test.

**5.1.2 Assembled Board Test** The method of test must be determined prior to design layout. If the defect rate is relatively high, most boards will require diagnosis, and the economics of automatic in-circuit test (ICT) will demand that full nodal access be provided within the board layout. If the defect rate is low, ICT may be omitted and rely on a functional test. Extremely low defect levels would theoretically allow 0 % nodal access (no bed-of-nails test at all), applying only a simple pass/no-pass test through a common interface connector.

The major considerations in determining nodal access are:

- Defect rate.
- Diagnostic capability.
- Real-estate impact.
- Board area.
- Layer count.
- Cost impact.

Determining the percentage of nodal access to design into a board layout requires trading off all the issues discussed previously: defect rate, test development cost, test operation costs including manual troubleshooting costs, and, of course, impacts on real estate. Short of having no defects at all, full nodal access remains the most desirable option.

As with through-hole technology boards, once the board is designed (nodal access fixed) and its tests are designed (test methods fixed), the defect rate becomes the primary key to reducing test costs. Therefore, defect reporting, analysis, and correction/prevention are imperative. This may involve closer supplier relationships to reduce component and board level problems, and in-house action to reduce process-induced problems.

**5.2 Nodal Access** In the early stages of product development cycles, test philosophies and strategies are often undefined. This is especially true when a company is moving from one level of packaging technology to the next higher level of packaging technology, for example, from through-hole technology to surface mount technology or from fine-pitch lead-frame packaged ICs to BGA or CSP. During these transition periods, the concurrent engineering approach is essential for designing nodal access for testability into the product. Concurrent engineering is the principle vehicle by which test priorities can and should be moved up to the beginning of the design cycle and addressed with a higher priority. In the early stages of a design, a test philosophy should be clearly defined, then a strategy for executing the tests can be implemented. An ideal philosophy to adopt is one that identifies all of the different test types and the level of test that each type requires.

**5.2.1 Test Philosophy** The test philosophy should be written to encompass whatever combination of tests are necessary for the product. Then, a simple strategy for implementing the required tests can be defined prior to beginning the design process. Planning testability at the beginning of a product development cycle instead of the end can result in significantly lower test costs per node and provide higher nodal accessibility throughout the entire process from initial design to final test.

The best test philosophy to adopt is one that will make provisions for executing every test method available. Even when the product testing procedure is well defined at the beginning of the development cycle, it may change after the design is complete. Some things to consider in outlining a test philosophy:

a) Strategic placement of all component vias.

b) Provide access to every node of every net.

c) Access of every node from one side of the board is preferred.

d) Correct test pad geometries and clearances.

Even in the higher density designs, the philosophy of providing 100% access to every node of every net from either side of the board can be accomplished. However, this decision must be made at the beginning of a design.

**5.2.2 Test Strategy for Bare Boards** After the product test philosophy has been established, a test strategy or procedure can be defined. For an overview of several elements of a procedure, consider the following:

a) Vision inspection of inner layers using AOI.

b) Vision inspection of O/L land/via connections.

c) Probe only vias on either side for bare board test.

d) Do not damage SMT lands with probe tips.

e) Probe secondary side vias for loaded test board.

f) Screen paste on vias for airtight board.

The actual product test strategy must be organized by all of the concurrent engineering team members who will be involved in the testing process. This will ensure that the integration of the various test types and procedures will not have too much redundancy, or create gaps that may endanger test integrity.

**5.3 Full Nodal Access for Assembled Board** The number of test probes needed to test the board is equal to the total number of device nodes or common connection between devices. However, in the case of most dense surface mount designs, this often requires the use of a double-sided, or clamshell test fixture because all of the nodes are not accessible from one side of the board.

In-Circuit Test (ICT) only needs to have access to one node per net. Every net has at least two nodes. Some nets have many nodes, for example, on memory boards one net may be connected to many nodes. In order to achieve full integrity at the ICT level, access to only one node of each net is all that is required. Therefore, the total number of test probes required to perform the ICT is significantly less than the number required for the bare board test.

For fine-pitch components, it is good design practice to distribute approximately half of the test vias to the inside of the land pattern and the other half to the outside of the land pattern as shown in Figure 5-1. This accomplishes two objectives:

1. The maximum density of test points established for a given piece of test equipment is not exceeded.
2. Wider distribution of test points reduces the high-pressure point areas which cause fixture bowing during vacuum or mechanical actuation.

**5.3.1 In-Circuit Test Accommodation** Specific via lands and holes can be reserved and accessed for automatic in-circuit test (ICT). The via land location for each common network in a circuit is matched to a test probe contact

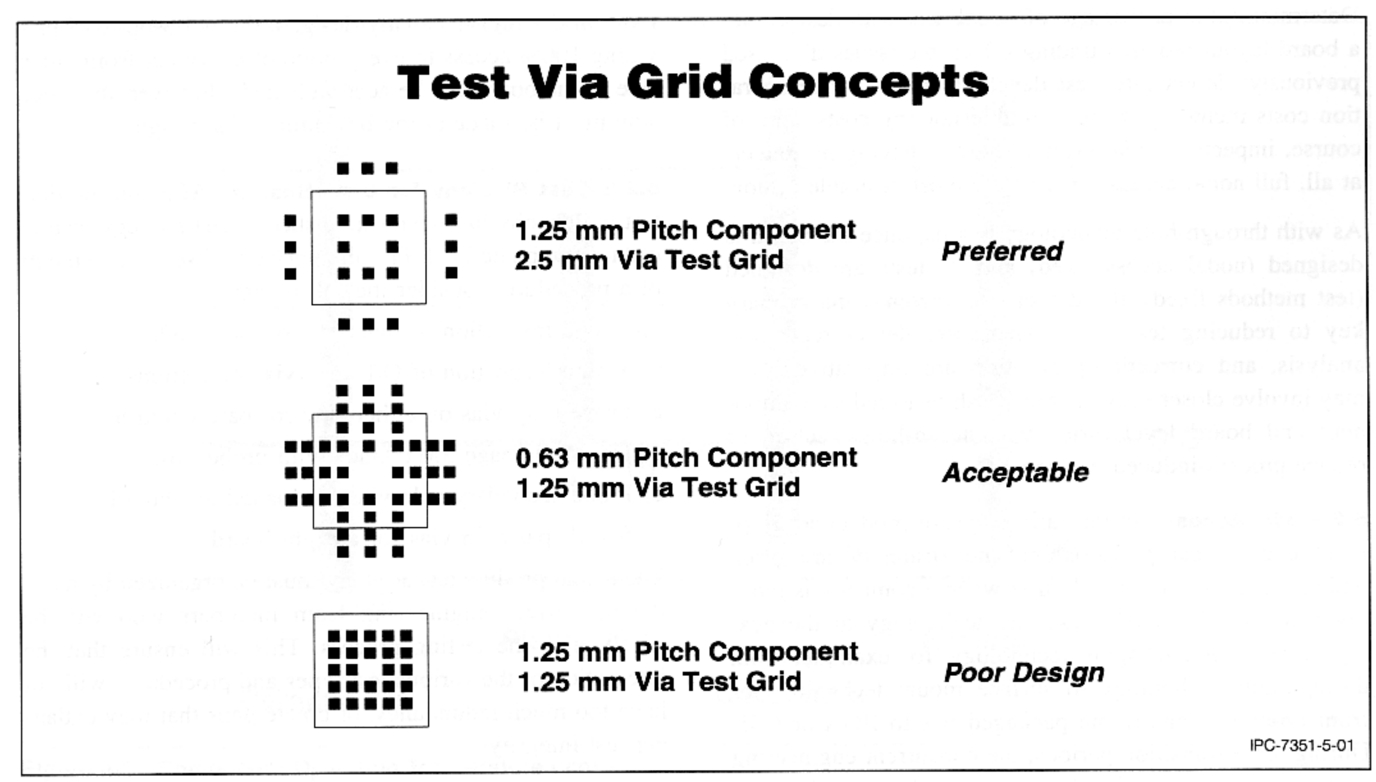



**Figure 5-1 Test Via Grid Concepts**

in the test fixture. The test system can then drive each device on the assembly and quickly locate defective devices or identify assembly process problems.

To insure precise alignment of the probe contact pins with the printed board, exact x and y probe position and specific networks must be furnished to the fixture developer. Identifying the test locations as components in the CAD database will allow for easy transfer of fixture drilling data. This data will reduce fixture development time and eliminate the drilling of excessive, nonfunctional holes in the fixture base. For low volume assembly, or high component density assembly, fixtureless testing by way of flying probe equipment is an option.

**5.3.2 Multi-Probe Testing** Some test probe systems can exert considerable deformation forces on the assembled boards and are a known source of premature service failures. An essential part of the printed board layout is to ensure that the location of probing points on the board are staggered at sufficient distances to avoid excessive deformation during multi-probe testing. When the probe point locations are highly concentrated, additional support may be needed in the test fixture design in order to counter the effect against the high probe pressure concentration. The area on the board where the support is to be provided should be located where it is clear of conductors and components.

**5.4 Limited Nodal Access** Provided the designer has allowed sufficient room for access to the test land(s), limited nodal access (less than 100%) still allows the use of spring probe (bed-of-nails) testing, but not as effectively as full nodal access does. When nodal access is less than 100%, shorts, defects and in-circuit testing cannot be performed completely, and some faults may not be detected.

A greater burden is therefore placed on functional or system test to detect and diagnose shorts, defects, and bad devices. This burden varies inversely with the nodal access percentage. The extra effort at functional test may consist of additional recurring manpower cost to diagnose failing boards, or it may mean developing a more detailed functional test (nonrecurring cost) than would have been planned otherwise.

**5.5 No Nodal Access** No nodal access (0%) prohibits bed-of-nails testing and defers all assembly defects and component testing until the functional or system test bed. This can only be cost-justified if the much higher cost-per-defect repair is performed so infrequently that the total cost is less than the cost of developing and operating an ATE bed-of-nails test. In other words, the first pass yields must be extremely high to justify this approach.

**5.6 Clam-Shell Fixtures Impact** Probing the printed board from both sides requires a "clam-shell" type of fixture. These are expensive, take more time to fabricate, require larger test lands on the primary side to protect against registration problems due to tolerance stack-ups, and they are more difficult to maintain.

### 5.7 Printed Board Test Characteristics

**5.7.1 Test Land Pattern Spacing** Design for testability is as much a part of the schematic design process as it is a part of the board layout process. Ideally, the printed board would have 100% of the nodes accessable from the secondary side of the PB assembly. In-circuit testers must have access to at least one node per net. Probe spacing is optional; however, standard probe spacing is typically 2.0 mm [0.0787 in] to 2.5 mm [0.0984 in] while miniature, needle type probes can be spaced as close as 1.0 mm [0.0394 in] to 1.25 mm [0.04921 in].

The drawbacks to the 1.0 mm [0.0394 in] to 1.25 mm [0.04921 in] grid-based test lands are the following. The miniature, needle type probes are more expensive and they do not hold up as well in high-volume production. Also, any via sites that are to be used as test points should be solder filled for better contact and increased probe life.

**5.7.2 Test Land Size and Shape** Lands or vias should be 0.9 mm [0.0354 in] to 1.0 mm [0.0394 in] for probing. As land sizes decrease, misses increase dramatically as shown in Figure 5-2. The use of square via lands may provide a larger target zone for the test probe to contact.

**5.7.3 Design for Test Parameters** The following other considerations are important to the general land pattern design that should be incorporated into the printed board.

a) Two unplated tooling holes should be available on diagonal corners of the printed board.

b) Test lands should be 2.5 mm [0.0984 in] minimum from the edge of the printed board to facilitate gasketing on vacuum fixtures.

c) When using vias for test points, caution should be taken to insure that signal quality is not degraded at the expense of testing capability.

d) Test lands should be 0.63 mm [0.0248 in] minimum from mounting land areas.

e) Where possible, provide numerous test lands for power and ground.

f) Where possible, provide test lands for all unused gates. Free running gates sometimes cause instability during in-circuit testing. This will provide a means of grounding these spurious signals.

It is sometimes desirable to provide drive and sense nodes test lands to perform six-wire bridge measurements during

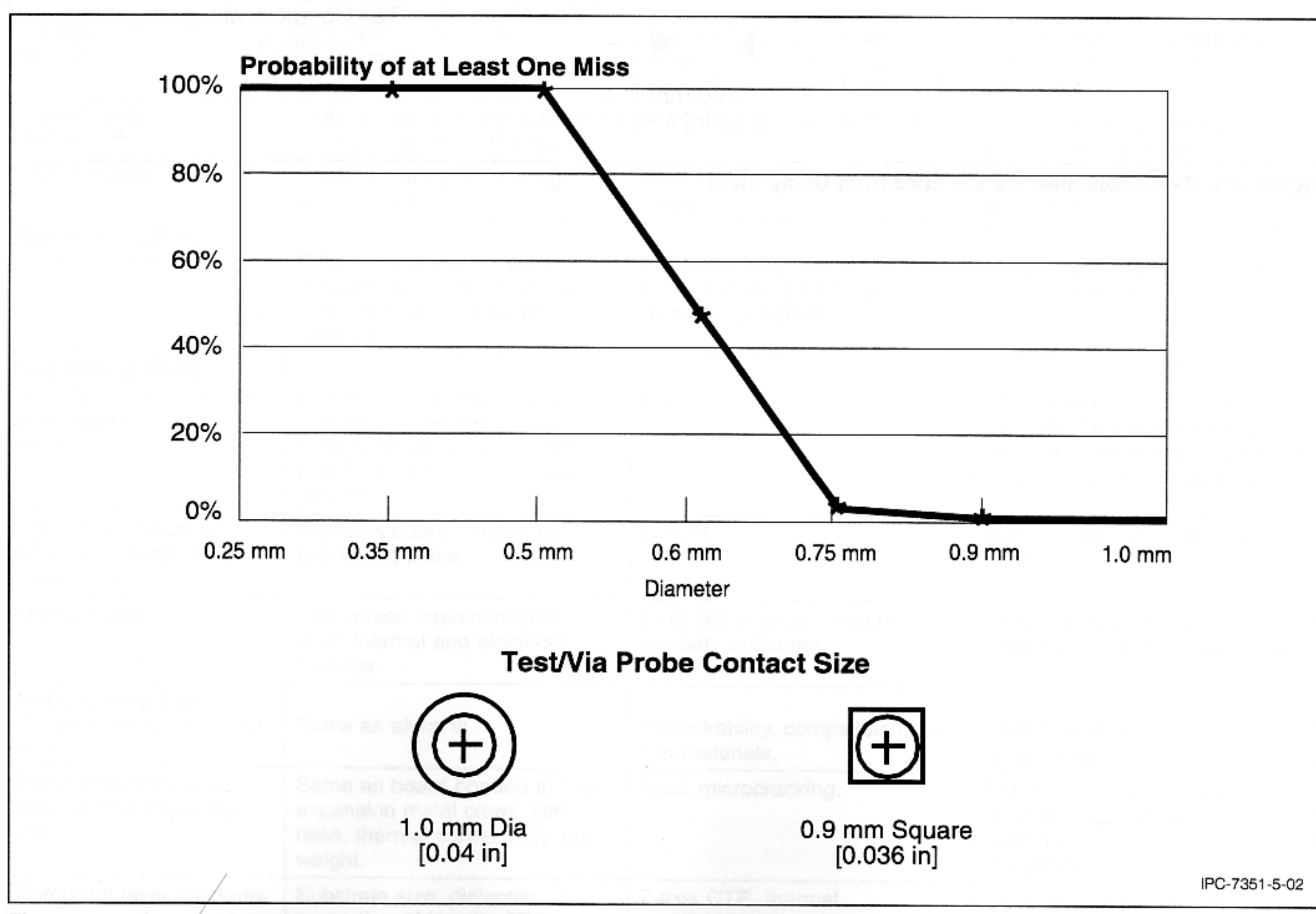



**Figure 5-2 General Relationship Between Test Contact Size and Test Probe Misses**

in-circuit test. Directions for this should come from test engineering.

In addition, it is useful to identify the test vias and lands on an assembly drawing in event of the need to modify the circuit topology. Changes made without moving test lands avoid fixture modification, saving cost and time.

Care should be taken when mounting components on the secondary side to avoid covering a via hole that is a designated test land. Also, if a via hole is too close to any component, damage may result to the component or fixture during probing (see Figure 5-3).

## 6 PRINTED BOARD STRUCTURE TYPES

The selection of a packaging and interconnecting structure for surface mounting applications is important for optimum thermal, mechanical and electrical systems reliability. Each candidate structure has a set of properties with particular advantages and disadvantages when compared to others (see Table 6-1).

It is probable that no one packaging and interconnecting structure or printed board will satisfy all of the needs of the application. Therefore, a compromise of properties should be sought that offers the best "tailoring" for component attachment and circuit reliability.

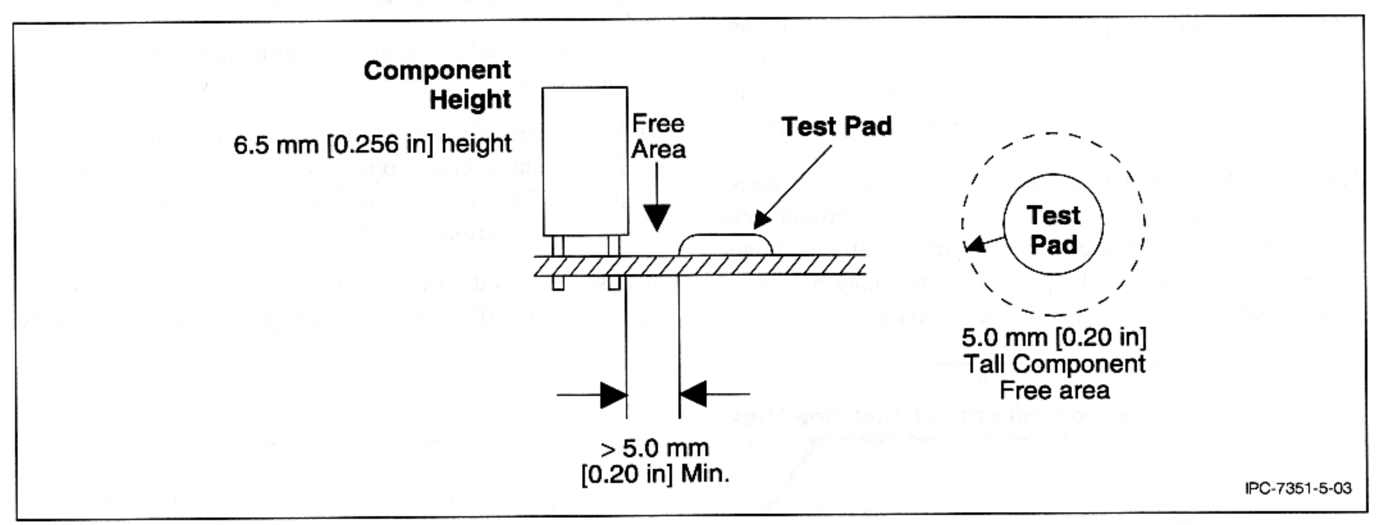



**Figure 5-3 Test Probe Feature Distance from Component**

**Table 6-1 Printed Board Structure Comparison**

| Type | Major Advantages | Major Disadvantages | Comments |
|---|---|---|---|
| **Organic Base Substrate**<br>Epoxy fiberglass | Substrate size, weight, reworkable, dielectric properties, conventional board processing. | Thermal conductivity, X, Y and Z axis CTE. | Because of its high X-Y plane CTE, it should be limited to environments and applications with small changes in temperatures and/or small packages. |
| Polyimide fiberglass | Same as epoxy fiberglass plus high temperatures X-Y axis CTE, substrate size, weight, reworkable, dielectric properties, high $T_g$. | Thermal conductivity, Z-axis CTE, moisture absorption. | Same as epoxy fiberglass. |
| Epoxy aramid fiber | Same as epoxy fiberglass, X-axis CTE, substrate size, lightest weight, reworkable, dielectric properties. | Thermal conductivity, Z-axis CTE, resin microcracking, Z axis CTE, water absorption. | Volume fraction of fiber can be controlled to tailor X-Y CTE. Resin selection critical to reducing resin micro-cracks. |
| Polyimide aramid fiber | Same as epoxy aramid fiber, X-axis CTE, substrate size, weight, reworkable, dielectric properties. | Thermal conductivity, Z-axis CTE, resin microcracking, water absorption. | Same as epoxy aramid fiber. |
| Polyimide quartz (fused silica) | Same as polyimide aramid fiber, X-Y axis CTE, substrate size, weight, reworkable, dielectric properties. | Thermal conductivity, Z-axis CTE, drilling, availability, cost, low resin content required. | Volume fraction of fiber can be controlled to tailor X-Y CTE, drill wear-out higher than with fiberglass. |
| Fiberglass/aramid composite fiber | Same as polyimide aramid fiber, no surface microcracks, Z axis CTE, substrate size, weight, reworkable, dielectric properties. | Thermal conductivity, X and Y axis CTE, water absorption, process solution entrapment. | Resin microcracks are confined to internal layers and cannot damage external circuitry. |
| Fiberglass/PTFE® laminates | Dielectric constant, high temperature. | Same as epoxy fiberglass, low-temperature stability, thermal conductivity, X and Y axis CTE. | Suitable for high-speed logic applications. Same as epoxy fiberglass. |
| Flexible dielectric | Light weight, minimal concern to CTE, configuration flexibility. | Size, cost, Z-axis expansion. | Rigid-flexible boards offer trade-off compromises. |
| Thermoplastic | 3-D configurations, low high-volume cost. | High injection-moulding setup costs. | Relatively new for these applications. |
| **Nonorganic Base**<br>Alumina (ceramic) | CTE, thermal conductivity, conventional thick film or thin film processing, integrated resistors. | Substrate size, rework limitations, weight, cost, brittle, dielectric constant. | Most widely used for hybrid circuit technology. |
| **Supporting Plane**<br>Printed board bonded to plane support (metal or nonmetal) | Substrate size, reworkability, dielectric properties, conventional board processing, X-Y axis CTE, stiffness, shielding, cooling. | Weight. | The thickness/CTE of the metal core can be varied along with the board thickness, to tailor the overall CTE of the composite. |
| Sequential processed board with supporting plane core | Same as board bonded to supporting plane. | Weight. | Same as board bonded to supporting plane |
| Discrete wire | High-speed interconnections, good thermal and electrical features. | Licensed process, requires special equipment. | Same as board bonded to low-expansion metal support plane. |
| **Constraining Core**<br>Porcelainized copper-clad invar | Same as alumina. | Reworkability, compatible thick film materials. | Thick film materials are still under development. |
| Printed board bonded with constraining metal core | Same as board bonded to low expansion metal cores, stiffness, thermal conductivity, low weight. | Cost, microcracking. | The thickness of the graphite and board can be varied to tailor the overall CTE of the composite. |
| Compliant layer sructures | Substrate size, dielectric properties, X-Y axis, CTE. | Z-axis CTE, thermal conductivity. | Compliant layer absorbs difference in CTE between ceramic package and substrate. |

**6.1 General Considerations** Printed board structures vary from basic printed wiring boards to very sophisticated supporting-core structures. However, some selection criteria are common to all structures. To aid in the selection process, Table 6-2 lists design parameters and material properties which affect system performance, regardless of PCB type. Also, Table 6-3 lists the properties of the materials most common for these applications.

**Table 6-2 PCB Structure Selection Considerations**

| Design Parameters | Material Properties | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Transition Temperatures | Coefficient of Thermal Expansion | Thermal Conductivity | Tensile Modulus | Flexural Modulus | Dielectric Constant | Volume Resistivity | Surface Resistivity | Moisture Absorption |
| Temperatures and power cycling | X | X | X | X | | | | | |
| Vibration | | | | X | X | | | | |
| Mechanical shock | | | | X | X | | | | |
| Temperatures and humidity | X | X | | | | X | X | X | X |
| Power density | X | | X | | | | | | |
| Chip carrier size | | X | | X | | | | | |
| Circuit density | | | | | | X | X | X | |
| Circuit speed | | | | | | X | X | X | |

**Table 6-3 PCB Structure Material Properties**

| Material | Material Properties | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Glass Transition Temperature | XY Coefficient of Thermal Expansion | Thermal Conductivity | XY Tensile Modulus | Dielectric Constant | Volume Resistivity | Surface Resistivity | Moisture Absorption |
| Unit of Measure | °C | PPM/°C (Note 4) | W/M°C | PSI x $10^{-6}$ | At 1 MHz | Ohms/cm | Ohms | Percent |
| Epoxy fiberglass | 125 | 13-18 | 0.16 | 2.5 | 4.8 | $10^{12}$ | $10^{13}$ | 0.10 |
| Polyimide fiberglass | 250 | 12-16 | 0.35 | 2.8 | 4.8 | $10^{14}$ | $10^{13}$ | 0.35 |
| Epoxy aramid fiber | 125 | 6-8 | 0.12 | 4.4 | 3.9 | $10^{18}$ | $10^{16}$ | 0.85 |
| Polyimide aramid fiber | 250 | 3-7 | 0.15 | 4.0 | 3.6 | $10^{12}$ | $10^{12}$ | 1.50 |
| Polyimide quartz | 250 | 6-8 | 0.30 | | 4.0 | $10^{9}$ | $10^{8}$ | 0.50 |
| Fiberglass/ Teflon® | 75 | 20 | 0.26 | 0.2 | 2.3 | $10^{10}$ | $10^{11}$ | 1.10 |
| Thermoplastic resin | 190 | 25-30 | | 3-4 | $10^{17}$ | $10^{13}$ | N/A | |
| Alumina-beryllia | N/A | 5-7 21.0 | 44.0 | 8.0 | $10^{14}$ | | | |
| Aluminum (6061 T-6) | N/A | 23.6 | 200 | 10 | N/A | 106 | | N/A |
| Copper (CDA101) | N/A | 17.3 | 400 | 17 | N/A | $10_6$ | | |
| Copper-clad Invar | N/A | 3-6 | 150XY/20Z | 17-22 | N/A | $10_8$ | | N/A |

**6.1.1 Categories** In general, a PCB structure will fit into one of four basic categories of construction: organic base material, nonorganic base material, supporting plane, and constraining core.

**6.1.2 Thermal Expansion Mismatch** A primary concern when using low expansion surface mount parts is the thermal expansion mismatch between the leadless part and the PCB structure. This mismatch will fracture solder joint interconnections if the assembly is subjected to thermal shock, thermal cycling, power cycling and high operating temperatures. The number of fatigue cycles before solder joint failure depends on the thermal expansion mismatch between the part and the PCB structure, the temperature range over which the assembly must operate, the solder joint thickness, the size of the part and the power cycling. For example, power cycling may cause an undesirable thermal expansion mismatch if a significant temperature difference exists between a device or package and the PB structure.

**6.2 Organic-Base Material** Organic-base materials work best with leaded chip carriers. With leadless chip carriers and some BGA packaging, the thermal expansion mismatch between package and substrate can cause problems. Also, flatness, rigidity, and thermal conductivity requirements may limit their use. Finally, attention should be paid to package size, I/O count, thermal cycling stability, maximum operating temperature and solder joint compliance.

**6.3 Nonorganic Base Materials** Nonorganic ceramic base materials typically used with thick- or thin-film technology, although more costly, are suited for leaded and leadless chip carrier designs. Suppliers can incorporate thick- or thin-film resistors directly on the ceramic structure and buried capacitor layers that increase density and improve reliability. However, repairability of the PCB structure is limited. Ceramic materials, usually alumina, appear ideal for PCB structure with leadless ceramic chip carriers because of their relatively high thermal conductivity. Unfortunately, the structure is limited to approximately 100 mm square. Ceramic PCB structures have three primary applications: ceramic hybrid circuits, ceramic multichip modules (MCM-L) and ceramic printed boards.

### 6.4 Alternative PCB Structures

**6.4.1 Supporting-Plane PCB Structures** Supporting metallic or nonmetallic planes can be used with conventional printed boards or with custom processing to enhance PCB properties. Depending on the results desired, the supporting plane can be electrically functional or not and can also serve as a structure stiffener, heatsink and/or CTE constraint.

**6.4.2 High-Density PCB Technology** High-density, sequentially processed, multilayer PCB structures are available in a wide variety of organic dielectrics. Using thinner copper foils for fabrication the board manufacturer can provide very narrow conductor and spacing features and by implementing smaller mechanical drills, laser ablation, photo-lithography or plasma processes, smaller blind and/or buried vias can be provided for layer-to-layer interconnections.

The major advantage of this system is that the vias can be as small as 0.10 mm [0.00394 in] or less and conductor widths can range from below 0.12 mm [0.00472 in] for high interconnection density. Thus, some applications can be satisfied with fewer signal layers while providing additional layers for power and ground. Refer to IPC-2226 for more detailed design guidelines for high density PCB.

**6.4.3 Constraining Core Structures** As with supporting plane, one or more supporting metallic or nonmetallic planes can serve as a stiffener, heatsink, and/or CTE constraint in constraining core structures.

**6.4.4 Porcelainized Metal (Metal Core) Structures** An integral core of low-expansion metal (for example, copper-clad Invar) can reduce the CTE of porcelainized metal structures so that it closely matches the CTE of the ceramic chip carrier. Also, the structure size is virtually unlimited. However, the low melting point of the porcelain requires low-firing-temperature conductor, dielectric and resistor inks.

## 7 ASSEMBLY CONSIDERATION FOR SURFACE MOUNT TECHNOLOGY (SMT)

The smaller size of surface mount components and the option of mounting them on one or both sides of the packaging and interconnecting structure reduces board real estate significantly. The type of SMT assembly is basically determined by the type of surface mount components to be used; see 7.1 for a description of types and classes.

**7.1 SMT Assembly Process Sequence** The SMT assemblies are soldered by reflow (infrared, hot air convection, laser, conduction, vapor phase, and/or wave soldering processes) depending upon the mix of surface mount and through-hole mount components. The process sequence for one-sided SMT is shown in Figure 7-1. Solder paste is applied, components are placed, the assembly is reflow soldered and cleaned. For two-sided SMT assemblies, the board is turned over and the process sequence just described is repeated. The assembly process for two-sided SMT is simply a sequential combination of SMT processes, however, component weight vs. surface tension should be calculated to determine if heavy components will require additional reinforcement prior to the second reflow soldering process.

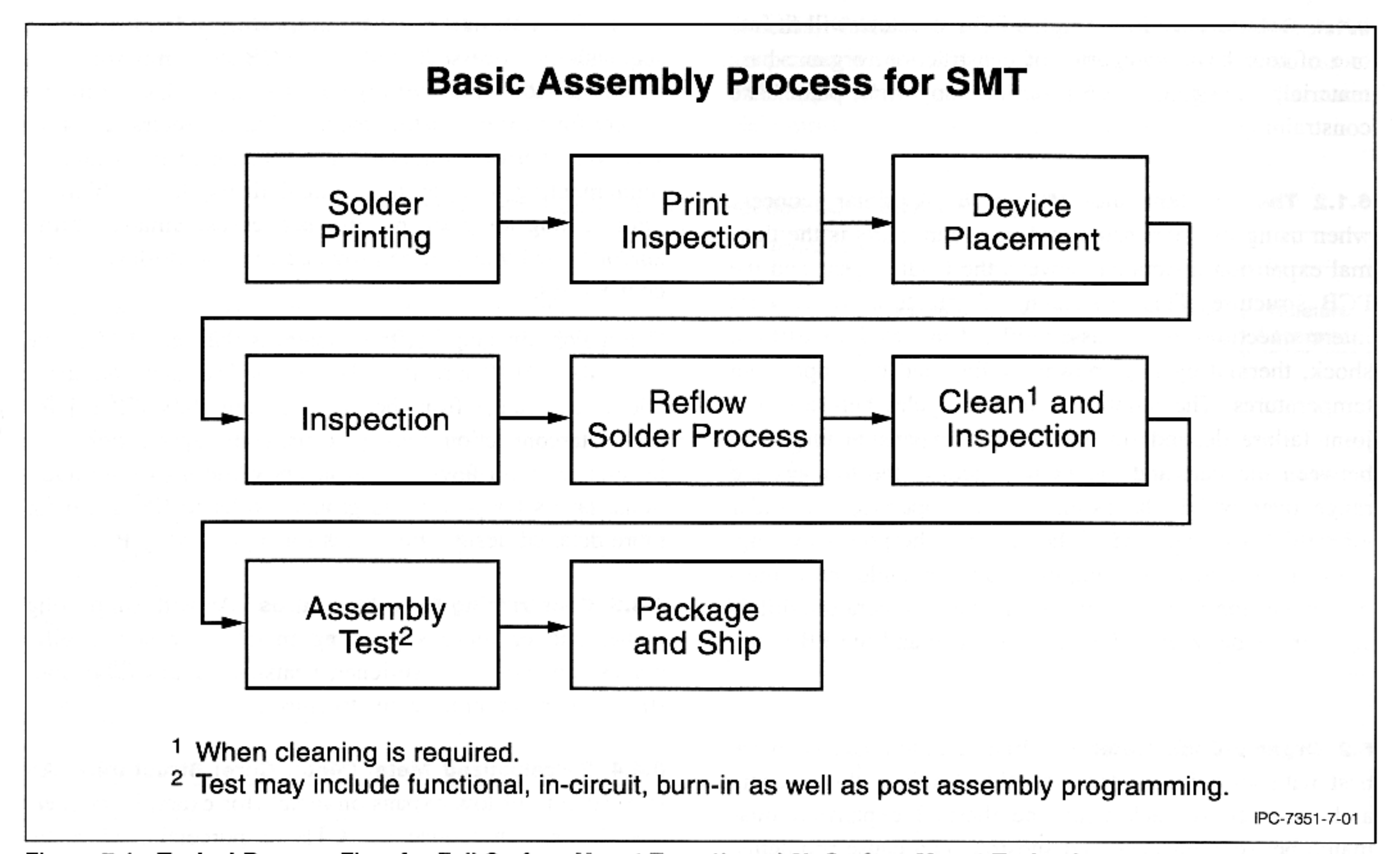



**Figure 7-1 Typical Process Flow for Full Surface Mount Type 1b and 2b Surface Mount Technology**

The process sequence for surface mount with through-hole or pin-in-hole (PIH) component technology is shown in Figure 7-2. Adhesive is applied and the surface mounted components placed. The adhesive is then cured, and the board is inverted to receive the through-hole component leads automatically or by hand insertion. After lead clinching (if required), and with the through-hole components on top and the surface mount components beneath, the board is typically wave soldered. An alternative sequence is to reverse the initial stages i.e., insert (and clinch) the through-hole components before attaching the surface mounted components and then wave soldering.

Finally the assembly may be cleaned, inspected, repaired if necessary, and tested, though not necessarily in that order.

## 7.2 Substrate Preparation

**7.2.1 Adhesive Application** In wave soldering surface mount components, selection and application of adhesive plays a critical role. With too much adhesive, the adhesive flows onto lands resulting in poor solder fillets. Too little adhesive will fail to accomplish its objective of holding parts to the bottom of the board during wave soldering.

**7.2.2 Conductive Adhesive** Some applications for SMT attachment use conductive adhesive as the attachment material. Unlike solder paste which is redistributed when reflowed, conductive adhesives must be properly controlled to ensure joint strength. Also, component placement must be controlled in order to prevent excessive adhesive squeeze-out, and possible shorts to adjacent lands.

**7.2.3 Solder Paste Application** Solder paste plays an important role in reflow soldering. The paste tacks the component before reflow. It contains flux, solvent, suspending agent, and alloy of the desired composition. Solder paste is applied on the lands before component placement either by screening, stenciling, or syringe. Screens are made from stainless steel or polyester wire mesh, and stencils are etched stainless steel, brass, and other stable alloys. Stencils are preferred for high-volume applications. They are more durable than screens, easier to align, and can be used to apply a thicker layer of solder paste, and, where narrow, point apertures are required for example, for fine-pitch lands. Electroformed stencils may be required for very small components such as 0201 capacitors and resistors.

The goal of the technology that's employed to make the stencil is to ensure that this transfer is as efficient and complete as possible. There are several post processes that enhance the stencil's performance, including electropolishing and trapezoidal section apertures that are created with laser cut technology

**7.2.3.1 Laser Cut Stencil Development** Laser cut stencils are produced directly from the customer's original Gerber file or GenCAM or IPC-2581 data. Eliminating the

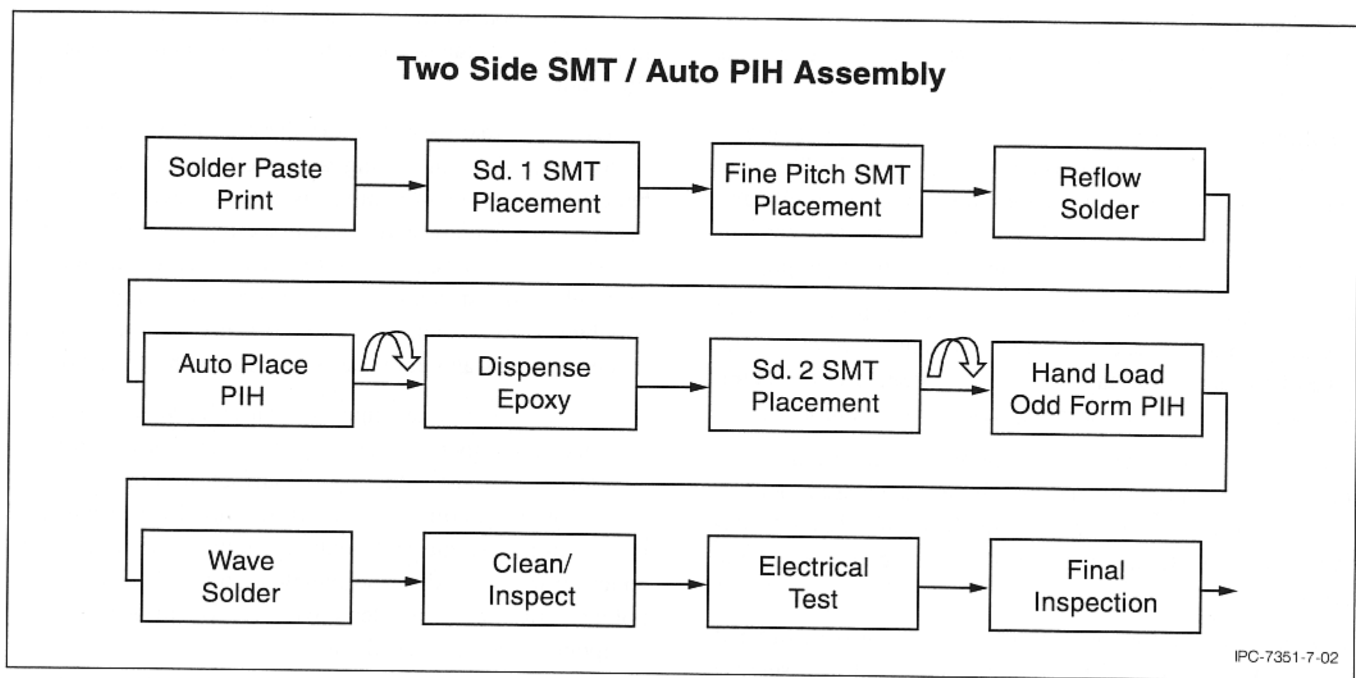



**Figure 7-2 Assembly Process Flow for Two-Side Surface Mount with PIH**

need to make a photo tool eliminates the potential for misregistration. And since there are no photographic steps, a stencil can be made with excellent positional accuracy and remake reproducibility. The tolerance on the aperture dimensions can be held to 7 µm [276 µin], allowing for printing 0.3 mm [0.0118 in] pitch. This process yields maximum paste release, resulting in minimal stencil cleaning, thereby increasing printing efficiency. Plus, the laser cutting process inherently creates trapezoidal apertures, furthering complete paste transfer.

A trapezoidal section aperture is one which has a larger opening on the contact (board) side of the stencil than on the squeegee side. The opening on the contact side is typically 5 µm [197 µin] per side larger than the squeegee side dimension, depending on the customer's requirements. This wall geometry, when further enhanced by electropolishing, allows for better paste release during the printing process. The results are more noticeable on fine pitch components.

Depending on the overall array design and given the right metal thickness selection, chem-etched stencils can perform adequately at 0.5mm [0.0197 in] pitch. Their efficiency can be improved with performance enhancing processes such as electropolishing and/or trapezoidal section apertures. For more details in the engineering of the stencil for specific soldering requirements, refer to IPC-7525.

**7.2.4 Solder Preforms** Solder preforms are sometimes used for through-hole mounted devices as well as SMT rework or prototype boards. They come in specific size and composition, with flux either inside the preforms, or as a coating or without flux. They may be cost-effective to avoid wave solder processes if there are only a few leaded components on the board.

**7.3 Component Placement** The accuracy requirements for device placement make it more practical to use robotically controlled machines for surface mount components on the board. Selection of the appropriate autoplacement machine is dictated by the type of components to be placed and the assembly production rate. Sequential placement equipment typically utilizes a software controlled X-Y moving table system. Components are individually placed on the printed board in succession. Typical cycle times vary with component size and complexity.

**7.3.1 Component Data Transfer** Prior to designing the PCB board in the CAD system, each component is constructed in digital form creating an electronic database. The CAD data is most often used to prepare photo-tool artwork, PCB fabrication details and assembly instructions but, if developed in the correct format, it can also be adapted to manufacturing processes. Direct transfer of CAD data into automated assembly systems will accelerate production set-up and reduce overall assembly system programming time.

When the CAD database for the device is prepared, specific physical data for each device can be used to assist assembly machine programming for both component placement (X-Y coordinate position) and orientation. To facilitate the X-Y coordinate information, a datum position must be established on the PW board surface. The recommended datum "0" for X and Y coordinates ideally, may be one of the global fiducial targets at the lower left or lower right corner of the board or panel. Surface mount devices are furnished in tape and reel as well as tube magazine feeders to accommodate high-speed assembly systems (tray carriers are most often adapted for fine-pitch components).

Each surface mount device is aligned using the body center and a starting orientation for reference. "0" degree is the basic orientation of the device.

Rotational data must be specified from the "0" position in a counter-clockwise direction (typically 90°- 180 - 270). The "0" starting position of the component is significant. Tape and reel and JEDEC tray packaged devices for example, have an established standard for orientation.

The tape-and-reel packaged devices have a predetermined orientation that is related to the perforated pattern on one edge of the embossed tape carrier. The standard orientation does vary, however, between unique device families.

Passive and active devices are supplied in a tape and reel format, held and protected within an embossed pocket. Each device family or package type has a standard orientation in relation to the perforated indexing pattern at the tape edge.

Orientation as well as polarity of a device must be defined in the CAD database if the output transferred to assembly systems is to be reliable. Resistors and capacitor devices are common in orientation and have no defined polarity. As the designer develops the component database, numbers are typically assigned to each end of the device to accommodate circuit routing and maintain orientation of value marking or polarity. Tantalum capacitors, diodes, ICs and other polarized components, for example, have unique orientation in relation to tape feed systems. Consider the relationship of the device orientation within the tape cavity to perforation at the tape carrier material edge.

**7.4 Soldering Processes** Like the selection of automated placement machines, the soldering process selection depends upon the type of components to be soldered and whether or not they will be used in combination with leaded parts. For example, if all components are surface mount types, reflow method (vapor phase, hot air convection or infrared) may be desirable. However, for through-hole and surface mount combinations, in mixed technology, a combination of wave soldering and reflow soldering may be used. No process is best for all soldering tasks. In addition, the number of soldering processes discussed in the following text are by no means complete.

**7.4.1 Wave Soldering** Wave soldering is an economical method of soldering mass terminations. There are five to six main process variables that must be controlled in the wave soldering process: fluxing, preheat, conveyor speed, conveyor incline, solder temperature, and possibly cooling rate.

In preheat, allowance in the conveyer system must be made for the thermal expansion of the board during preheating and soldering to prevent board warpage.

In fluxing, flux density, activity and flux foam/flux spray/ flux wave height must be closely monitored. A system must be in place to determine when the flux activity has deteriorated and when the old flux must be replaced and the new flux added.

Speed is the time sequence and duration of all of the steps in soldering. By controlling the speed, more uniform and better joints result. In controlling the conveyer speed, preheating a packaging and interconnecting assembly in two or three stages minimizes the thermal shock damage to the assembly and improves its service life. Uniform preheating is achieved by developing a solder schedule that specifies preheat settings and conveyer speed for each type of board.

The solder wave is an important variable. Wave geometry is especially important for preventing icicles and bridges and for the proper soldering of surface mounted components. Wave geometries include uni-directional and bi-directional; single and double; rough, smooth and dead zone; oil intermix, dry, and bubbled, and with or without a hot air knife. Special solder waves just for surface mounted components are also available.

The concern generally expressed in wave soldering of surface mount devices is damage to the components when they go through the soldering wave at 260 °C [500 °F]. The maximum shift in tolerance of resistors and capacitors is generally found to be 0.2%. This is a negligible amount considering the part tolerance of commonly used components is 5% to 20%. The components generally spend about three seconds in the wave but they are designed to withstand soldering temperatures of 260 °C [500 °F] for up to ten seconds.

In wave soldering, outgassing and solder skips are two other main concerns. The outgassing or gas evolution occurs on the trailing terminations of chip resistors and capacitors. It is believed to be caused by insufficient drying of flux and can be corrected by raising the packaging and interconnecting assembly preheat temperature or time. The other concern, solder skips, is caused by the shadow effect of the part body on the trailing terminations. Orienting the part in such a way that both terminations are soldered simultaneously solves most shadow effect problems. Some manufacturers use an extra land to serve as a "solder thief" for active components.

The most common method for solving both outgassing and shadow effect is by switching to the dual wave system where the first wave is turbulent and the second wave is laminar. The turbulent wave serves to provide an adequate amount of solder across the surface of the packaging and interconnecting structure in order to help eliminate outgassing and solder skips. The laminar wave is used to help eliminate icicles and bridging.

**7.4.2 Vapor Phase (VP) Soldering** Vapor phase soldering, also known as condensation soldering, uses the latent heat of vaporization of an inert liquid for soldering. The

latent heat is released as the vapor condenses on the part to be soldered. The soldering temperature is constant and is controlled by the type of fluid.

Unlike wave, IR, convection and laser soldering, vapor phase soldering does not require control of the heat input to the solder joints or to the board. It heats independently of the part geometry, heats uniformly, and does not exceed the fluid boiling temperature. This process is also suitable for soldering odd-shaped parts, flexible circuits, and pins and connectors, as well as for reflow of tin-lead electroplate and surface mount packages. Since heating is by condensation, the rate of temperature rise depends on the mass of the part. Therefore, the leads on the package in contact with the packaging and interconnecting structure heat up faster than the component body. This may lead to wicking of the solder up the lead. Before exposing the loaded assembly to VP reflow process, preheating the assembly is highly recommended to avoid thermal shock to components and the PCB.

**7.4.3 IR Reflow Soldering**

In infrared (IR) reflow soldering, the radiant or convective energy is used to heat the assembly. There are basically two types of IR reflow methods, either focused (radiant) or nonfocused (convective). The latter is proving more desirable for SMT. The focused IR radiates heat directly on the parts and may unevenly heat assemblies. The heat input on the part may also be color-dependent. In nonfocused or diffused IR, the heating medium can be air or an inert gas or simply the convection energy. A gradual heating of the assembly is necessary to drive off volatiles from the solder paste. After an appropriate time in preheat, the assembly is raised to the reflow temperature for soldering and then cooled.

**7.4.4 Hot Air/Gas Convection Soldering** The reflow process affects soldering by transporting the boards through a stream of heated gas (e.g., air, nitrogen). Heat is transferred to the components and board by conduction from the gas. Because the boards do not receive significant direct radiation from the heating source, convection soldering avoids the shadowing problems that can occur with infrared soldering machines, especially short wavelength (lamp) versions. This enables more uniform heating and a higher component density on the board compared to other mass reflow soldering methods. The gas temperature controls the maximum temperature that can be seen by the assembly.

Use of a nitrogen atmosphere permits better thermal coupling between the circulating gas and the component terminations. In addition to improved wetting, the process window for double-sided reflow is enlarged, and lower activated solder paste flux can be used.

**7.4.5 Laser Reflow Soldering** Laser soldering complements other mass soldering processes rather than replacing them and, as with in-line reflow soldering, lends itself well to automation. It is faster than hand soldering but not as fast as wave, vapor, IR soldering or hot air convection. Heat-sensitive components that may be damaged in reflow processes can be soldered by laser. Process problems include thermal damage to surrounding areas and solder balls.

**7.4.6 Conduction Reflow Soldering** Conduction reflow affects soldering through the transference of heat from beneath the PCB. This can have advantages with high mass components, temperature sensitive components and metal backed assemblies. In comparison with other solder processes, the slightly slower heating and cooling ramp times caused by heat spreading through the PCB substrates can provide a reduction of thermal shock and improved resistance against rapid cooling issues such as tombstoning. Though in-line conduction reflow ovens are available, the most common use of conductive reflow is in "hot plate" rework systems.

For more detail regarding reflow soldering refer to IPC-7530.

**7.5 Cleaning** Flux requiring solvent cleaning—synthetic or rosin-based fluxes are generally known as synthetic activated (SA), synthetic mildly activated (SMA), rosin activated (RA) or rosin mildly activated (RMA). Stabilized halogenated hydrocarbon/alcohol azeotropes are the preferred solvents for removal of synthetic and rosin-based flux residues.

**7.6 Repair/Rework** The repair/rework of surface mount assemblies requires special care in design and practice. Because of the small land geometries, heat applied to the board should be minimized. There are various tools available for removing components. Resistance heating tweezers are usually used for removing surface mounted components. Various types of hot air/gas and IR systems are also used for removing surface mounted components. One of the main issues when using hot air/gas devices is preventing damage to adjacent components. Refer to IPC-7711/21. There are four basic requirements for a successful rework; good printed board design layout, selection of the correct rework equipment or tools, sufficient manual skill, and adequate training.

Successful removal of large multi-leaded integrated circuit packages involves the use of hot gas or heated electrode tools. Sufficient clearance around the package to permit the re-work is essential. Clearance should be provided completely around the device as identified in the standards as the "courtyard manufacturing zone."

**7.6.1 Heatsink Effects** Large ground planes or heatsinks will conduct heat away from the component being reworked if present in a printed board substrate. Extra heat,

perhaps for longer periods, is then required which, in turn, can lead to damage to components or the board. The fact that the solder joints may not reach reflow temperature is no guarantee that the component or the board have not been overheated. Heatsinking effects is a design problem which must be tackled at the printed board layout stage. Whenever possible, any component termination which may not rework, including leaded-through hole type, should be thermally isolated from any ground plane or integral heat-sink by a short length of copper conductor.

**7.6.2 Dependence on Printed Board Material Type** To ensure minimum damage to the printed board during rework, base laminate should be a good quality resin and reinforcement type from a high copper peel strength material. High packing density is required. The use of inferior laminates can easily lead to problems with lands peeling away during rework. This may result in either scrapping of complete assemblies or expensive repair of damaged copper area. For boards having high thermal mass such as middle-core types or those with large area ground planes, to avoid employing a tool with high heat input rate, the use of a hot plate to provide background heating is essential.

**7.6.3 Dependence on Copper Land and Conductor Layout** The space on a board is at a premium or single conductors must be kept very short. Designers will often route a conductor between adjacent device land space at a pitch of the component device being placed. In such cases, conductors should be covered with a soldermask to minimize the risk of lifting conductors during rework operations.

Routing conductors between lands at 1.0 mm pitch and below increases the risk of damage to the conductors during the rework operation. For more detail regarding development, planning and trouble shooting the steps involved in the process of producing surface mount assemblies, refer to IPC-S-816.

## 8 IPC-7352 DISCRETE COMPONENTS

Discrete components are generally purchased in 8 mm and 12 mm wide tape and reel (see Figure 8-1). EIA-481 is the applicable specification for tape and reel. Consult your manufacturers guide for the packaging availability of your component.

Parts susceptible to damage by electrostatic discharge shall be supplied in a manner that prevents such damage. Tape peel strength shall be 40 grams ± 30 grams. Peel from the top for the top cover of the tape. Reel materials used in the construction of the reel shall be easily disposable metal, chip board, styrene plastic or equivalent. Reels shall not cause deterioration of the components or their solderability. Reels must be able to withstand high humidity conditions.

Parts must be capable of withstanding cleaning processes currently used by board assembly manufacturers. This may include as a minimum four-minute exposures to solvent cleaning solutions at 40 °C [104 °F], plus a minimum of a one-minute exposure to ultrasonic immersion at a frequency of 40 kHz and a power of 100 watts per square foot. Alkaline systems in use shall also not damage parts or remove markings.

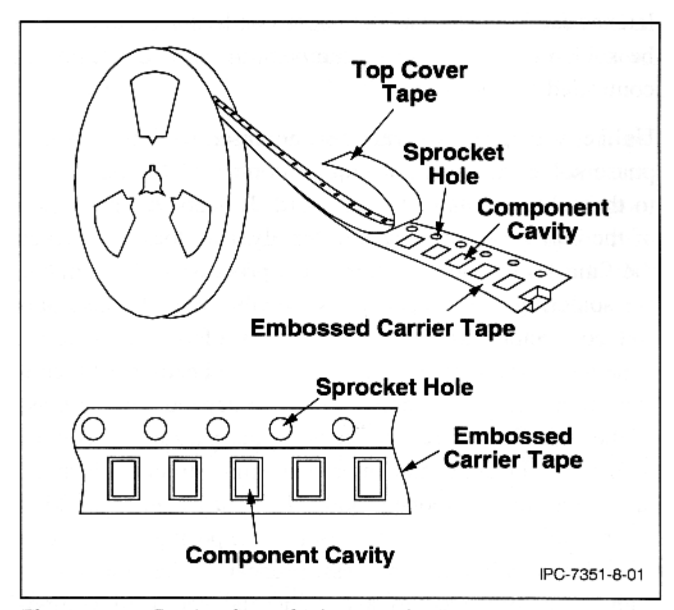



**Figure 8-1 Packaging of Discrete Components**

End terminations should be solder coated with a tin/lead alloy or a lead free equivalent. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a postplating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules, lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

For lead free finishes a combination of tin, silver and copper is the prevalent replacement for the tin/lead finish. Solderability testing should be applied per IPC-J-STD-002 to determine attachment capability of the applicable component type.

The following sections for each component family provide information on basic component construction, termination materials, marking, carrier package format and resistance to soldering.

**8.1 Chip Resistors (RESC)** A variety of values exist for resistors. This section describes the most common types.

**8.1.1 Basic Construction** The resistive material is applied to a ceramic substrate and terminated symmetrically at both ends with a "wrap around" metal U-shaped band. The resistive material is face-up, thus trimming to close tolerances is possible. Since most equipment uses a vacuum-type pickup head, it is important that the surface of the resistor is made flat after trimming, otherwise vacuum pickup might be difficult (see Figure 8-2).

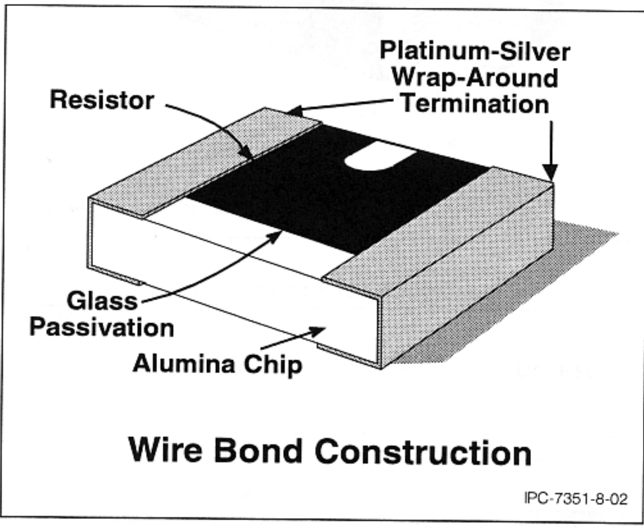



**Figure 8-2 Chip Resistor Construction**

**8.1.2 Marking** Resistors equal to or larger than 2012 [0805] are labeled. Resistors smaller than 1608 [0603] are generally unlabeled.

**8.1.3 Carrier Package Format** Bulk rods, 8 mm tape/4 mm pitch is preferred for best handling. Tape and reel specifications provide additional requirements.

**8.1.4 Resistance to Soldering** Parts should be capable of withstanding five cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C [500 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

**8.2 Chip Capacitors (CAPC)** A variety of values exist for capacitors. This section describes the most common types.

**8.2.1 Basic Construction** Multilayer ceramic capacitors use substrate materials such as alumina for hybrid circuits and porcelainized metal. The monolithic construction used in producing these chips results in a solid block of ceramic with an enclosed electrode system and metallized ends for circuit attachment. This solid block is rugged and capable of withstanding the harsh environment and treatment associated with manufacturing processes (see Figure 8-3). Electrodes are given a common terminal by coating the chip ends with a precious metal-glass formulation suspended in an organic vehicle. Consecutive drying and firing eliminates the organic components and affects a bond between the ceramic dielectric and glass constituent in the termination.

**8.2.2 Marking** Ceramic capacitors are typically unmarked.

**8.2.3 Carrier Package Format** Bulk rods, 8 mm tape/4 mm pitch is preferred for best handling. Tape and reel specifications provide additional requirements.

**8.2.4 Resistance to Soldering** Parts should be capable of withstanding five cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C [500 °F].

Caution should be exercised when using the 4564 [1825] capacitor mounted on organic substrates due to CTE mismatch if the assembly sees wide temperature swings in the assembly process or end use. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

**8.3 Inductors (INDC, INDM, INDP)** A variety of values exist for inductors. This section describes the most common types.

**8.3.1 Basic Construction** At the time of publication, there was no industry standard document for leadless inductors. The dimensions were taken from manufacturer's catalogs, but only when at least two component vendors manufacture the same package. However, the same inductor value may not be available in the same package from the two manufacturers (see Figure 8-4).

**8.3.2 Marking** Parts are available with or without marked inductance values.

**8.3.3 Carrier Package Format** Bulk rods, 8 mm tape/4 mm pitch is preferred for best handling. Tape and reel specifications provide additional requirements.

**8.3.4 Resistance to Soldering** Parts should be capable of withstanding five cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C [500 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

**8.4 Tantalum Capacitors (CAPT)** A variety of values exist for tantalum capacitors. This section describes the most common types.

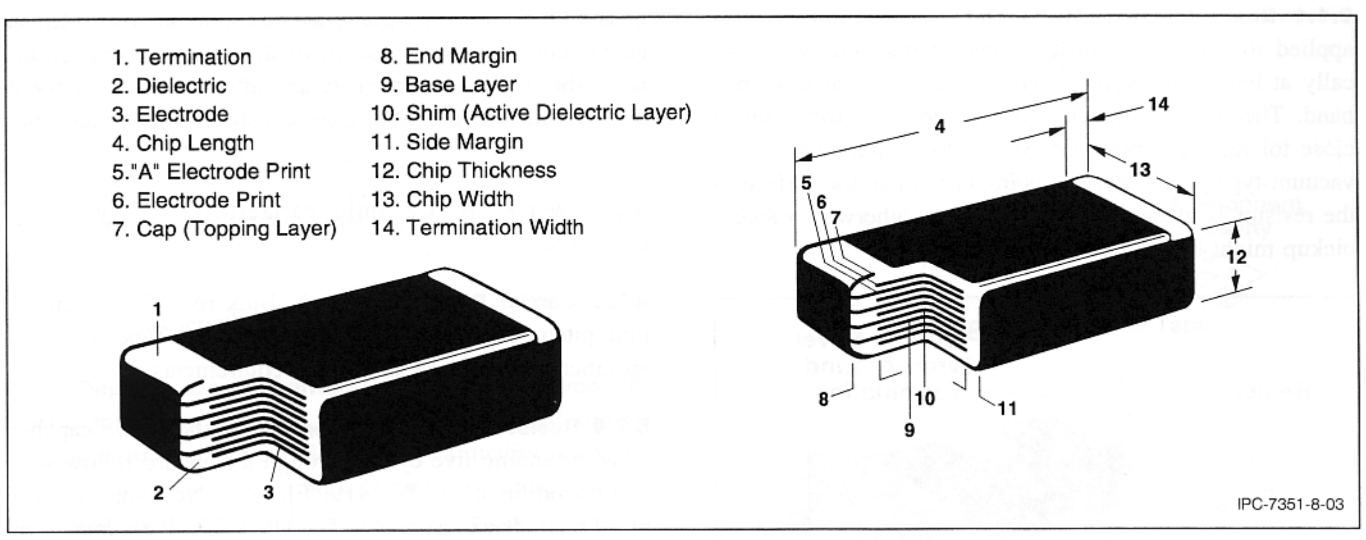



**Figure 8-3 Chip Capacitor Construction**

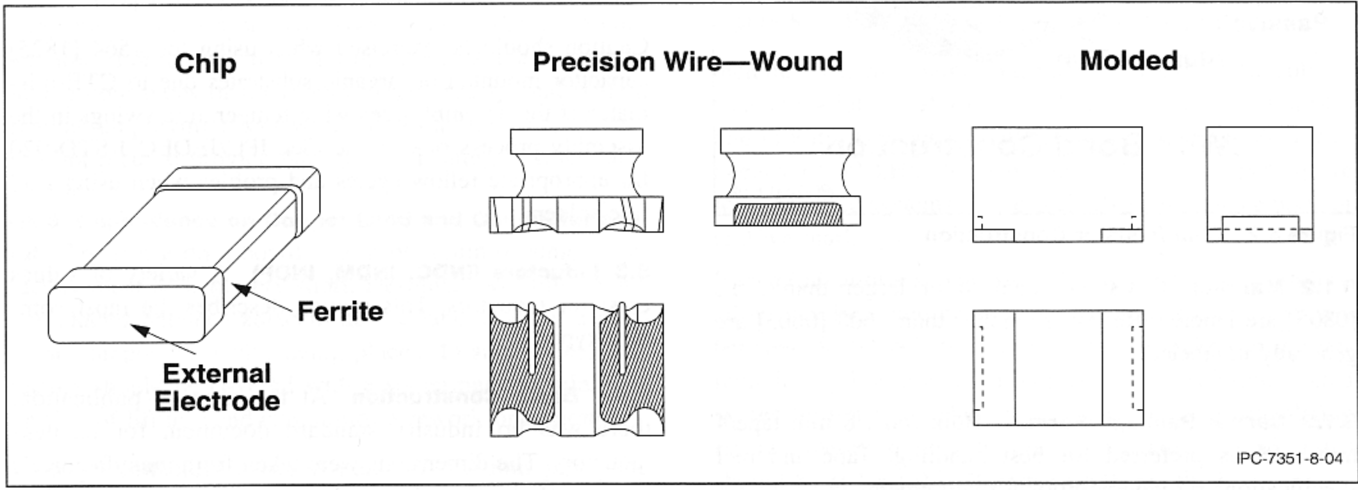



**Figure 8-4 Inductor Construction**

**8.4.1 Basic Construction** See Figure 8-5.

**8.4.2 Marking** Parts are available with or without marked capacitance values.

**8.4.3 Carrier Package Format** Bulk rods, 8 mm tape/4 mm pitch is preferred for best handling. Tape and reel specifications provide additional requirements.

**8.4.4 Resistance to Soldering** Parts should be capable of withstanding five cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C [500 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

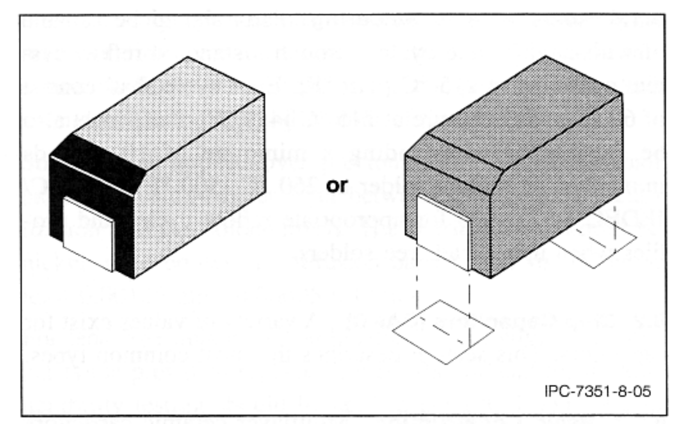



**Figure 8-5 Tantalum Capacitor Construction**

**8.5 Metal Electrode Face Diodes (DIOMELF, RESMELF)** Resistors, ceramic capacitors, and tantalum capacitors may all be packaged in these tubular shapes.

**8.5.1 Basic Construction** See Figures 8-6 and 8-7.

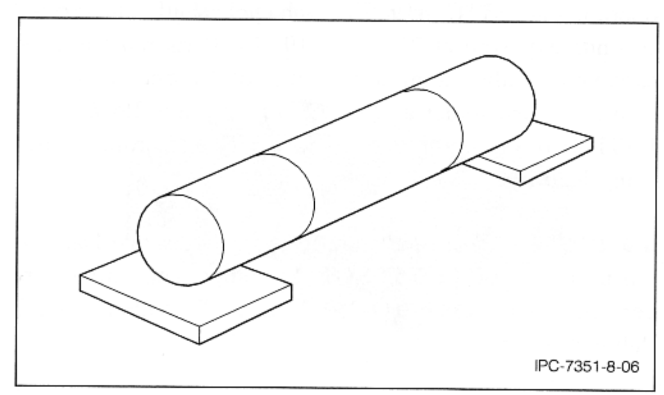



**Figure 8-6 Metal Electrode Face Component Construction**

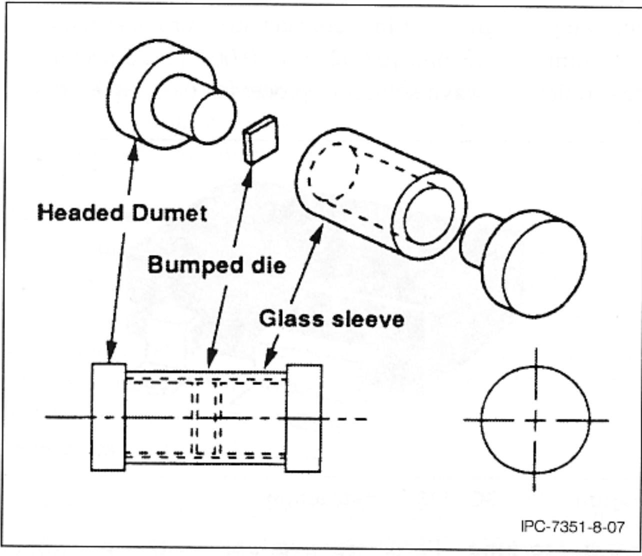



**Figure 8-7 Break-Away Diagram of MELF Components**

**8.5.2 Marking** Parts are available with or without marked values.

**8.5.3 Carrier Package Format** Bulk rods, 8 mm tape/4 mm pitch is preferred for best handling. Tape and reel specifications provide additional requirements.

**8.5.4 Resistance to Soldering** Parts should be capable of withstanding five cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C [500 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

**8.6 SOT23** One of the first active devices in packaged form for surface mounting was the SOT device. Plastic encapsulated three terminal devices with leads formed out from the body were surface mounted to overcome some of the problems and difficulties in handling dip transistors. In general, SOT packages are used with diodes, transistors, and small I/O devices. The SOT 23 package is the most common three-lead surface mount configuration.

**8.6.1 Basic Construction** The SOT 23 package has had several redesigns to meet the needs of both hybrid and printed board surface mount industries. These changes resulted in low, medium and high profile characteristics which basically reflect the clearance that the body is from the mounting surface. See Figure 8-8 for construction characteristics.

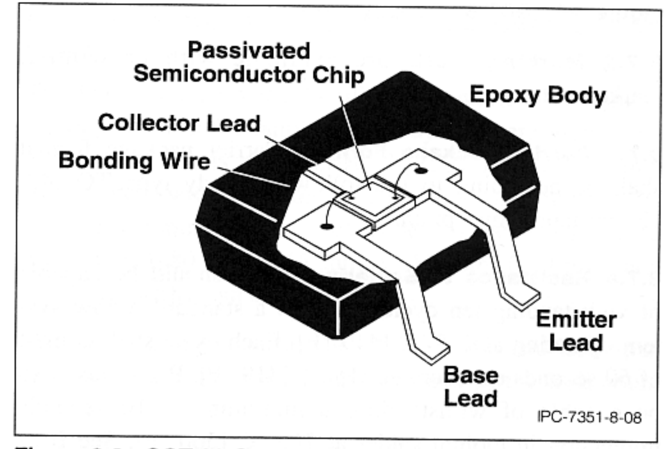



**Figure 8-8 SOT 23 Construction**

**8.6.2 Marking** Parts are available with or without marked values.

**8.6.3 Carrier Package Format** Carrier package format shall be according to the following: body type TO-236, 8 mm tape/4 mm pitch.

**8.6.4 Resistance to Soldering** Parts should be capable of withstanding five cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C [500 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

**8.7 SOT89** These parts are for high power transistors and diodes. These parts are used where heat transfer to a supporting structure is important. IPC-7352 SOT89 component outlines are derived from outline TO-243 Issue "C" within JEDEC Publication 95.

**8.7.1 Basic Construction** See Figure 8-9. The SOT 89 package dimensions are designed to meet the needs of both the hybrid and printed board surface mount industries. In

order to provide an adequate heat transfer path, there is no clearance between the body of the component and the packaging and interconnect structure. This design may accommodate the reflow or wave soldering processes.

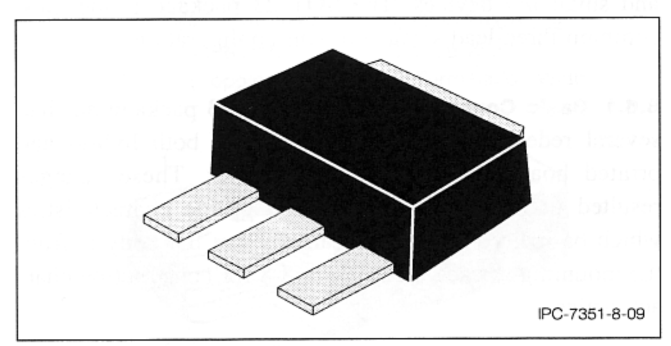



**Figure 8-9 SOT 89 Construction**

**8.7.2 Marking** Parts are available with or without marked values.

**8.7.3 Carrier Package Format** Carrier package format shall be according to the following: body type TO-243, 12 mm tape/8 mm pitch.

**8.7.4 Resistance to Soldering** Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C [500 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

**8.8 SOD123** IPC-7352 SOD123 component outlines are derived from outline DO-214 "Issue B" within JEDEC Publication 95.

**8.8.1 Basic Construction** The small outline diode comes in two configurations. One is a gullwing-leaded (SOD123) configuration as shown in Figure 8-10. The other is a molded configuration with terminations (DIOSMB).

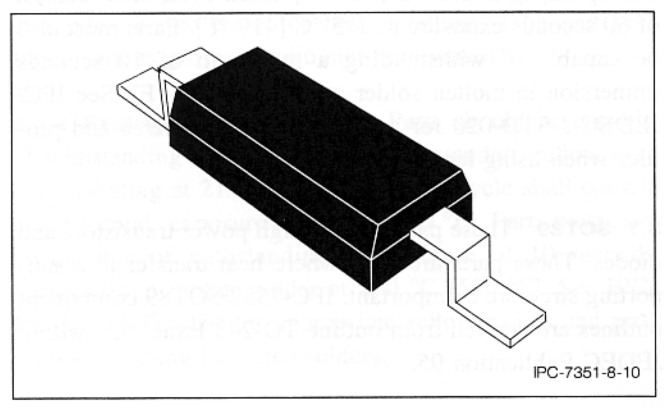



**Figure 8-10 SOD 123 Construction**

**8.8.2 Marking** Parts are available with or without marked values.

**8.8.3 Carrier Package Format** Carrier package formats are tape and reel; 12 mm tape/8 mm pitch.

**8.8.4 Resistance to Soldering** Parts should be capable of withstanding 10 cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C [500 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

**8.9 SOT143** These parts are for dual diodes and Darlington transistors. IPC-7352 SOT143 component outlines are derived from outline TO-253 "Issue C" within JEDEC Publication 95.

**8.9.1 Basic Construction** The dimensional characteristics are designed to meet the needs of the surface mount industry. The clearance between the body of the component and the packaging and interconnect structure is specified at 0.05 mm to 0.13 mm [0.002 in to 0.005 in] to accommodate reflow or wave soldering processes (see Figure 8-11).

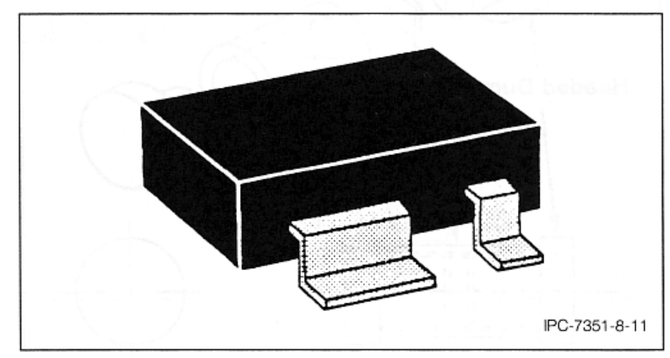



**Figure 8-11 SOT143 Construction**

**8.9.2 Marking** Parts are available with or without marked values.

**8.9.3 Carrier Package Format** Carrier package format shall be according to the following: body type TO-253, 8 mm tape/4 mm pitch.

**8.9.4 Resistance to Soldering** Parts should be capable of withstanding five cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C [500 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

**8.10 SOT223** These parts are for dual diodes and Darlington transistors. IPC-7352 SOT223 component outlines are derived from outline TO-261 "Issue C" within JEDEC Publication 95.

**8.10.1 Basic Construction** The dimensional characteristics are designed to meet the needs of the surface mount industry. The clearance between the body of the component and the packaging and interconnect structure is specified at 0.06 mm [0.00236 in] (basic) to accommodate reflow or wave soldering processes (see Figure 8-12).

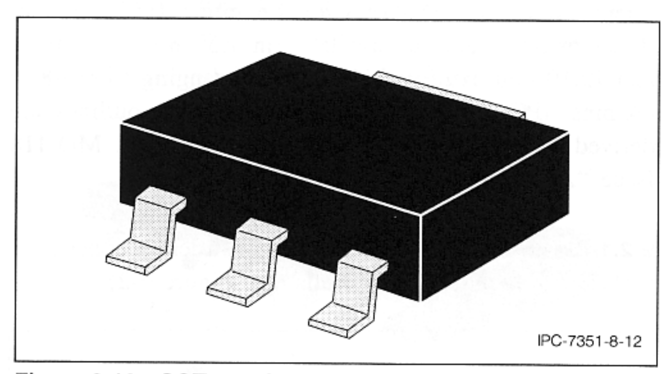



**Figure 8-12 SOT 223 Construction**

**8.10.2 Marking** Parts are available with or without marked values.

**8.10.3 Carrier Package Format** Carrier package format shall be according to the following: body type TO-261, 12 mm tape/8 mm pitch.

**8.10.4 Resistance to Soldering** Parts should be capable of withstanding five cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C [500 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

**8.11 TO252 (DPAK Type)** These parts are for dual diodes and Darlington transistors. IPC-7352 TO252 component outlines are derived from outline TO-252 "Issue B" within JEDEC Publication 95.

**8.11.1 Basic Construction** See Figure 8-13.

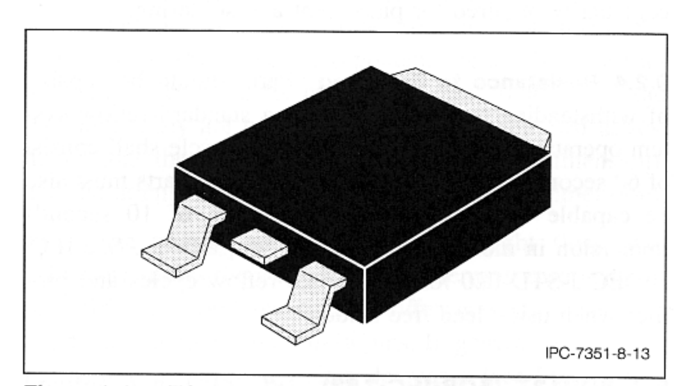



**Figure 8-13 TO252 (DPAK Type) Construction**

**8.11.2 Marking** Parts are available with or without marked values.

**8.11.3 Carrier Package Format** Carrier package format shall be according to the following: body type TO-252, 12 mm tape/8 mm pitch.

**8.11.4 Resistance to Soldering** Parts should be capable of withstanding five cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C [500 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

### 8.12 Molded Body Diode (DIOSMB)

## 9 IPC-7353 GULLWING LEADED COMPONENTS, TWO SIDES

The two-sided gullwing family has a number of generic package sizes in the family. The body sizes are varied, but the basic family is characterized by 1.27 mm or 0.63 mm lead centers with leads on the long side of a rectangular body. The family has been expanded to include a limited number of 0.80 mm, 0.65 mm, 0. 50 mm, 0.40 mm, and 0.30 mm pitch devices.

Within the component families, body width and lead span are constant, while body length changes as the lead count changes.

A major advantage of this package style is that it can be pretested prior to substrate assembly while still offering relatively high density. Its small area, low height, and minimal weight are its major advantages over DIPs. The package has orientation features on the edge of the package to aid in handling and identification.

Coplanarity is an issue for all components with gullwings on two sides. In general, the leads must be coplanar within 0.1 mm. That is, when the component is placed on a flat surface, (e.g., a granite block), no lead may be more than 0.1 mm off the flat surface.

**Note:** Some members of the SOIC family are processed on the secondary side and wave soldered. When parts are processed by wave solder, correct part orientation must be observed. Consult your manufacturer before placing SOICs on the wave solder side of the board.

High lead count packages and fine pitch parts, 0.63 mm or less, should be processed by infrared reflow, conduction reflow, or hot bar soldering, and should not be wave soldered.

End terminations should be solder coated with a tin/lead alloy or a lead free equivalent. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a postplating

reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

For lead free finishes a combination of tin, silver and copper is the prevalent replacement for the tin/lead finish. Solderability testing should be applied per IPC-J-STD-002 to determine attachment capability of the applicable component type.

**9.1 SOIC** These small outline integrated circuits (SOIC) are all on 1.27 mm pitch, and are available in 4.0 mm narrow body, 7.50 mm or 7.60 mm wide body and 9.02 mm extra wide body sizes, ranging from 8 to 36 pins. IPC-7353 SOIC component outlines are derived from outlines MS-012, MS-013, MO-110 and MO-120 within JEDEC Publication 95.

**9.1.1 Basic Construction** Basic construction consists of a plastic body and metallic leads (see Figure 9-1).

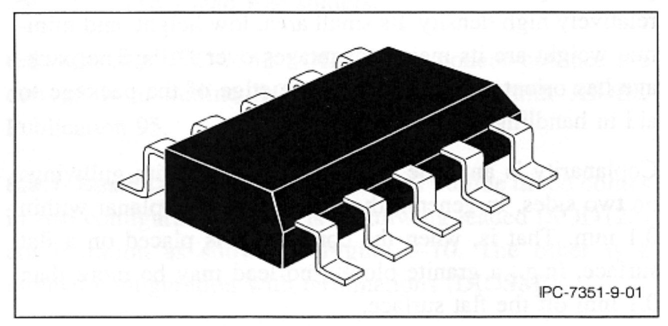



**Figure 9-1 SOIC Construction**

**9.1.2 Marking** All parts shall be marked with a part number and "Pin 1" location. "Pin 1" location may be molded into the plastic body.

**9.1.3 Carrier Package Format** Carrier packaging format may be provided in a tray carrier, but tape and reel carriers are preferred for best handling and high volume applications. Bulk packaging is not preferred because of lead coplanarity required for placement and soldering.

**9.1.4 Resistance to Soldering** Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C [500 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

**9.2 SOP8/SOP63 (SSOIC)** These shrink small outline integrated circuits (SSOIC) are on either 0.635 mm or 0.80 mm pitch, and are available in 7.59 mm wide body and 12.10 mm extra wide body sizes, ranging from 48 to 64 pins. IPC-7353 SOP8/SOP63 component outlines are derived from outlines MO-117 Issue "A" and MO-118 Issue "A" within JEDEC Publication 95.

**9.2.1 Basic Construction** Basic construction consists of a plastic body and metallic leads (see Figure 9-2).

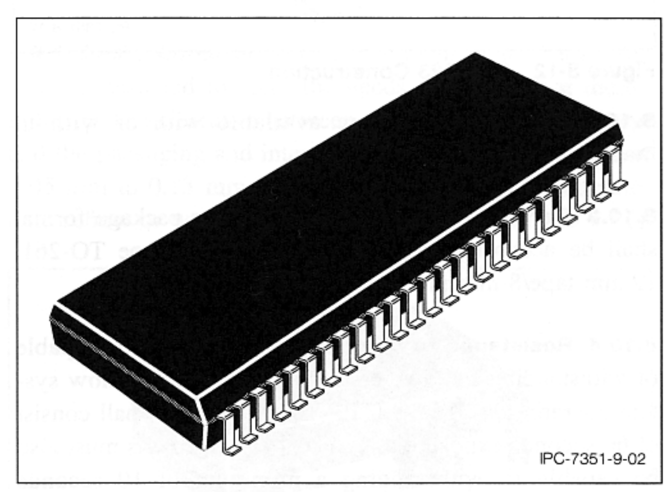



**Figure 9-2 SOP8/SOP63 Construction**

**9.2.2 Marking** All parts shall be marked with a part number and "Pin 1" location. "Pin 1" location may be molded into the plastic body.

**9.2.3 Carrier Package Format** Carrier packaging format may be provided in a tray carrier, but tape and reel carriers are preferred for best handling and high volume applications. Bulk packaging is not preferred because of lead coplanarity required for placement and soldering.

**9.2.4 Resistance to Soldering** Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C [500 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

**9.3 SOP127 (SOP-IPC-782)** IPC-7351 has defined center-to-center spacing for these land patterns slightly differently than is indicated in the EIAJ specification EIAJ-7402-1.

This standard allows for 6 families of the SOP127. EIAJ classifies the families by the center-to-center distance of the land patterns and the outer extremities of the leads (dimension "L" in IPC-7351). The basic construction of the SOP127 specified by EIAJ is the same construction as for SOIC specified by JEDEC. Both have gullwing leads on 1.27 mm centers. The EIAJ specification allows for a number of positions of the components to be in any of the families (e.g., body width) (see Figure 9-3).

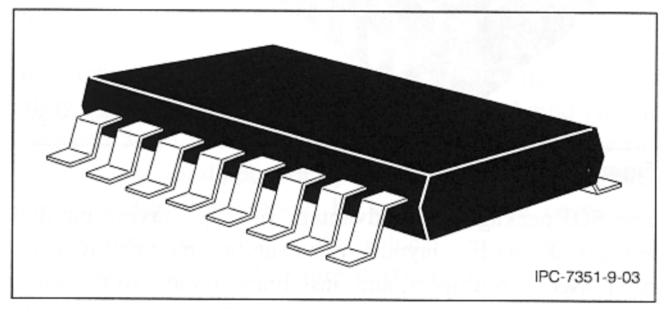



**Figure 9-3 SOP127 Construction**

**9.3.1 Marking** Parts are available with or without part number markings. Usually an index mark indicates pin 1.

**9.3.2 Carrier Package Format** Carrier packaging format may be provided in a tray carrier, but tape and reel carriers are preferred for best handling and high volume applications. Bulk packaging is not preferred because of lead coplanarity required for placement and soldering.

**9.3.3 Resistance to Soldering** Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C [500 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

**9.4 TSSOPS** The thin shrink small outline package (TSSOP) is unique among the component families of this section because its leads protrude from the short side of the plastic body. The TSSOP components are available in four different pitches: 0.30 mm, 0.40 mm, 0.50 mm, and 0.65 mm. They are typically specified by their two largest dimensions-the plastic body size (in the short dimension), and the nominal toe-to-toe length (in the long dimension).

Their use has grown because their height (less than 1.27 mm) allows them to be used in memory card technology. IPC-7351 outlines sixteen different body sizes with pin counts ranging from 16-76 pins. In general, as the long dimension increases, the pitch decreases (see Figure 9-4).

**9.4.1 Marking** Parts are available with or without part number markings. Usually an index mark indicates pin 1.

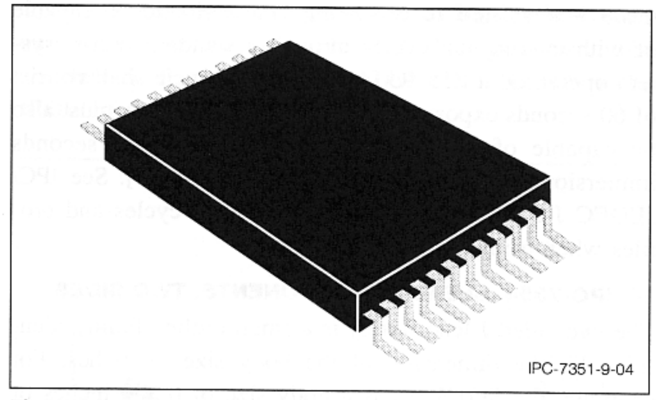



**Figure 9-4 TSSOP Construction**

**9.4.2 Carrier Packages Format** Trays are usually used for handling TSSOPs.

**9.4.3 Resistance to Soldering** Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C [500 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

**9.5 CFP127** See Figure 9-5 for an example of a ceramic flat pack (CFP127). Basic construction consists of a ceramic body and metallic leads. Leads are trimmed and formed into gullwing shape and all are on 1.27 mm centers. IPC-7353 CFP127 component outlines are derived from outlines MO-003, MO-004, MO-018, MO-019, MO-020, MO-021, MO-022 and MO-023 within JEDEC Publication 95.

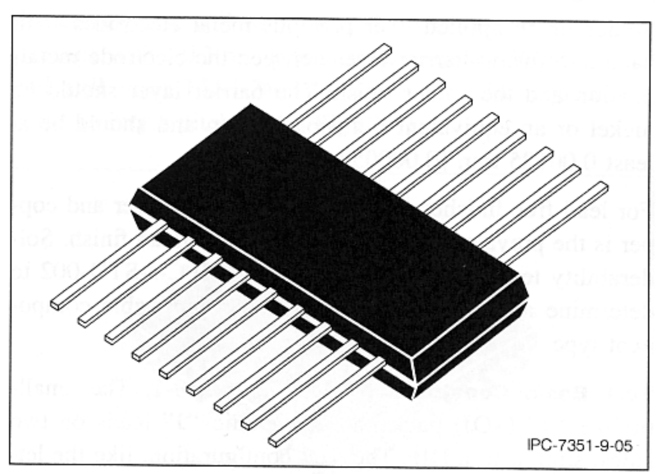



**Figure 9-5 CFP127 Construction**

**9.5.1 Marking** All parts shall be marked with a part number and an index area. The index area shall identify the location of pin 1.

**9.5.2 Carrier Packages Format** Carrier trays are used for handling CFPs.

**9.5.3 Resistance to Soldering** Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C [500 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

## 10 IPC-7354 J-LEADED COMPONENTS, TWO SIDES

The two-sided J lead family is a small outline family identified by the dimension of the body size in inches. For example, the SOJ/300 has a body size of 0.300 inches or 7.63 mm, the SOJ/350 has a body size of 0.350 inches or 8.88 mm, the SOJ/400 has a body size of 0.400 inches or 10.12 mm, and the SOJ/450 has a body size of 0.450 inches or 11.38 mm. Package lead counts range from 14 to 28 pins. IPC-7354 SOJ component outlines are derived from outlines MO-061, MO-063, MO-065, MO-077, MO-088, MS-027, and MS-091 within JEDEC Publication 95.

End terminations should be solder coated with a tin/lead alloy or a lead free equivalent. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a postplating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

For lead free finishes a combination of tin, silver and copper is the prevalent replacement for the tin/lead finish. Solderability testing should be applied per IPC-J-STD-002 to determine attachment capability of the applicable component type.

**10.1 Basic Construction** See Figure 10-1. The small-outline "J" (SOJ) package has metallic "J" leads on two sides, similar to a DIP. The lead configuration, like the letter J, extends out the side of the plastic body package and bends under the package forming a J bend. The point of contact of the lead to the land pattern is at the apex of the J bend and is the basis for the span of the land pattern.

The leads must be coplanar within 0.1 mm. That is, when the component is placed on a flat surface, no lead may be more than 0.1 mm off the flat surface.

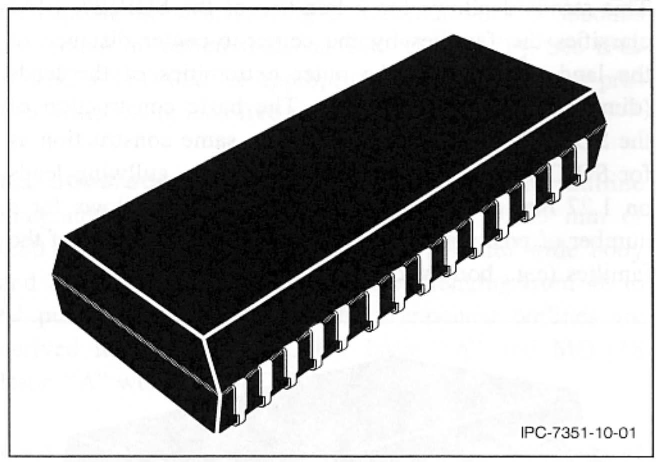



**Figure 10-1 SOJ Construction**

The SOJ package takes advantage of chips having parallel address or data line layouts. For example, memory IC's are often used in multiples, and buss lines connect to the same pin on each chip. Memory chips in SOJ packages can be placed close to one another because of the parallel pin layout and the use of "J" leads. With high capacity memory systems, the space savings can be significant.

**10.2 Marking** The SOJ family of parts is generally marked with manufacturers' part numbers, manufacturers' name or symbol, and a pin 1 indicator. Some parts may have a pin 1 feature in the case shape instead of pin 1 marking. Additional markings may include date code/manufacturing lot and/or manufacturing location.

**10.3 Carrier Package Format** Components may be provided in tube or tape packaging. Tape is preferred for best handling and high volume applications. Bulk packaging is not acceptable because of lead coplanarity requirements required for placement and soldering. EIA-481 provides details on tape requirements.

**10.4 Process Considerations** J lead packages are normally processed using standard solder reflow processes. Parts should be capable of withstanding 10 cycles through a standard reflow system operating at 215°C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215°C [419 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

## 11 IPC-7355 GULL-WING LEADED COMPONENTS, FOUR SIDES

The four-sided gull-wing family is characterized by gull wing leads on four sides of a square or rectangular package. The family includes both molded plastic and ceramic case styles. The acronyms PQFP (Plastic Quad Flat Pack), BQFP (Bump Quad Flat Pack), SQFP (Shrink Quad Flat Pack), QFPR (Quad Flat Pack, Rectangular) and CQFP (Ceramic Quad Flat Pack) are also used to describe the family.

There are several lead pitches within the family from 1.27 mm down to 0.30 mm. High lead-count packages are available in this family that accommodate complex, high lead-count chips.

The four sided gull-wing families of parts are generally marked with manufacturer part numbers, manufacturer name or symbol, and a pin 1 indicator. Some parts may have a pin 1 feature in the case shape instead of pin 1 marking. Additional markings may include date code/ manufacturing lot and/or manufacturing location.

End terminations should be solder coated with a tin/lead alloy or a lead free equivalent. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a postplating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

For lead free finishes a combination of tin, silver and copper is the prevalent replacement for the tin/lead finish. Solderability testing should be applied per IPC-J-STD-002 to determine attachment capability of the applicable component type.

Four-sided gull-wing families are usually processed using standard solder reflow processes. Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. High lead-count fine pitch parts may require special processing outside the normal pick/place and reflow manufacturing operations. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

All parts shall be marked with a part number and an index area. The index area shall identify the location of pin 1.

**Note:** Four sided gull-wing packages are normally processed by solder reflow operations. High lead-count fine pitch parts may require special processing outside the normal pick/place and reflow manufacturing operations.

Separate pick/place, excise, and reflow processes are sometimes used as an alternate to normal SMT processes.

**11.1 BQFP (PQFP)** See Figure 11-1. BQFPs have leads on a 0.635 mm pitch. IPC-7355 BQFP component outlines are derived from outlines MO-069 and MO-086 within JEDEC Publication 95.

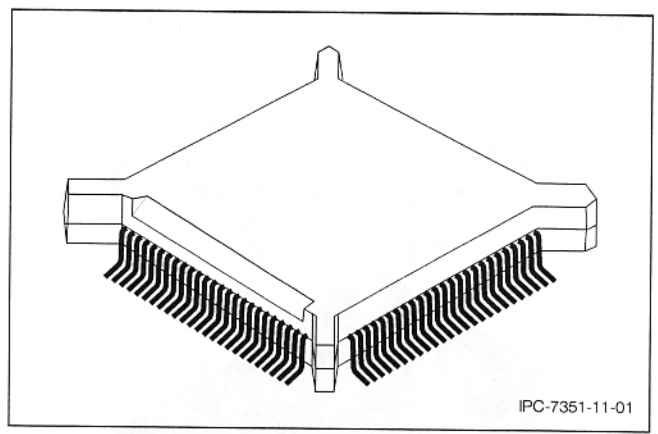



**Figure 11-1 BQFP Construction**

**11.1.1 Carrier Package Format** The carrier package format for BQFPs is the tube format; however, packaging trays provide the best handling capability.

**11.2 SQFP/QFP** The shrink quad flat pack (SQFP) has been developed for applications requiring low height and high density. The SQFP, along with the TSOP components, are frequently used in memory card applications. The square SQFP/QFP family has leads on a 0.80 mm, 0.65 mm, 0.63 mm, 0.50 mm, 0.40 mm, or 0.30 mm pitch. IPC-7355 SQFP/QFP component outlines are derived from outline MO-108 within JEDEC Publication 95.

Two different pin counts are allowed for each package and the component will still meet the standard (e.g., a 5x5 package with a 0.3 mm pitch can have either 56 or 48 pins, and still meet EIAJ-7404-1). QFPs are also square and come in larger pitches (see Figure 11-2).

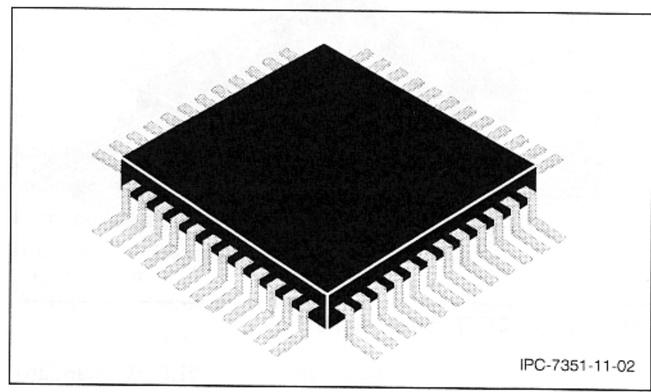



**Figure 11-2 SQFP and QFP Construction**

**11.2.1 Carrier Package Format** The carrier package format for flatpacks may be tube format; but, in most instances, flatpacks are delivered in a carrier tray.

**11.3 QFPR** The quad flat pack, rectangular (QFPR) has been developed for applications requiring low height and high density. The QFPR, along with the TSOP components, are frequently used in memory card applications. The QFPR family has leads on a 0.80 mm, 0.60 mm, 0.50 mm, 0.40 mm, or 0.30 mm pitch. IPC-7355 QFPR component outlines are derived from outline MO-108 within JEDEC Publication 95 (see Figure 11-3). Two different pin counts are allowed for each package and the component will still meet the standard (e.g., a 5x5 package with a 0.3 mm pitch can have either 56 or 48 pins, and still meet EIAJ-7404-1).

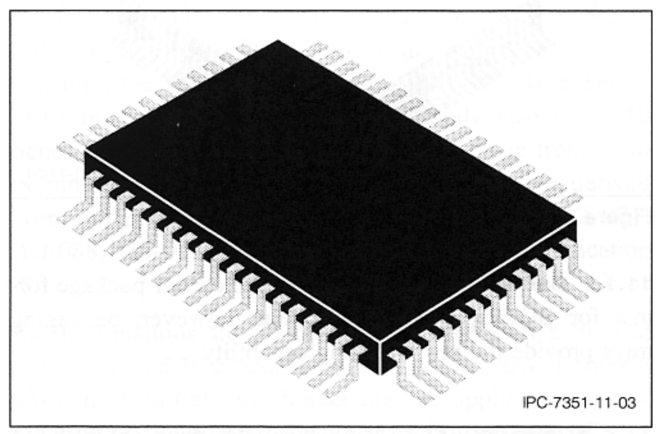



**Figure 11-3 QFPR Construction**

**11.3.1 Carrier Package Format** The carrier package format for flat packs may be tube format; but, in most instances, flat packs are delivered in a carrier tray.

**11.4 CQFP** See Figure 11-4 for ceramic quad flat pack (CQFP) construction. Leaded ceramic chip carriers are typically supplied with an open cavity for chip placement. Ceramic or metal lids are soldered, epoxied, or attached with glass frit around the cavity to provide a hermetic seal.

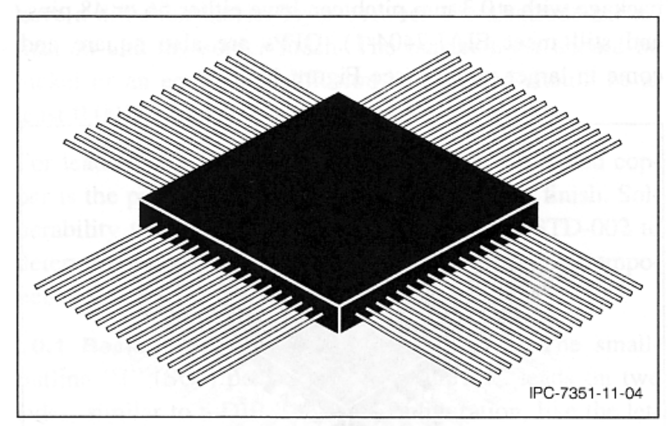



**Figure 11-4 CQFP Construction**

An exception to this construction is the JEDEC standard outline MS-044, which has the chip bonded to a lead frame, which is then sealed between two ceramic bodies with glass frit, similar to CERDIP fabrication. The ceramic packages are available in 28- through 196-lead configurations, with 1.27 mm, 0.80 mm, and 0.63 mm center spacing. Aside from the MS-044 exception, IPC-7355 CQFP component outlines are derived from outlines MO-084, MO-104 and MO-114 within JEDEC Publication 95.

Preleaded ceramic chip carriers typically have copper alloy or Kovar leads that are attached by the manufacturer. Leads are typically bonded to metallization on the top surface of the chip carrier. However, leads can be attached to the package castellations as well. Brazing or thermo-compression bonding is usually the attachment means. Preleaded packages using lead-frame construction are also available. These chip carriers have ceramic bodies with two opposing halves which mate above and below a lead frame to which the chip has been previously bonded. The seal is preformed with glass frit.

Leads can be formed to different shapes, such as "J," "L," or "C" configurations. Leads bent in the "L" configuration are known as "gullwings."

Preleaded chip carriers may be supplied with leads straight and attached to a common strip. The user must detach the common strip and form the leads to the desired configuration. This is done to minimize lead bending during shipping and handling. Leads may be supplied pretinned or with gold plating, as is often done for packages intended for a high reliability user.

**11.4.1 Carrier Package Format** Tube carriers are preferred for best handling.

## 12 IPC-7356 J LEADED COMPONENTS, FOUR SIDES

Four-sided J-Lead components, also known as Leaded Chip Carriers, are either ceramic or plastic packages with terminations which extend beyond the package outlines. These terminations typically space the body of the package from the packaging and interconnect structure for reasons of cleaning, inspecting, or accommodating differences in thermal expansion. The leads may be attached to the package body either before or after chip attachment.

In plastic leaded chip carriers, the primary packaging distinction concerns the point in which a chip is incorporated into the package. A premolded package is supplied as a leaded body with an open cavity for chip attachment. A postmolded body part typically has the chip attached to a lead frame with an insulating plastic body molded around the assembly. It is supplied from the manufacturer without apertures.

Leaded ceramic chip carriers may be similarly classified, but with a difference in category. The distinction concerns the point at which leads, if desired, are attached to the ceramic body. A preleaded ceramic chip carrier is supplied with copper or Kovar leads brazed to metallization integral with the ceramic package. Typically, the package is supplied with an open cavity for chip attach. A metal or ceramic lid is epoxied, soldered, or attached with glass frit

to provide a hermetic seal around the chip. After these steps, the leaded assembly is attached to the printed board.

A postleaded ceramic chip carrier typically has leads soldered to metallization on the ceramic package after chip attachment. These leads may take the form of edge clips or solder columns. Incorporation of leads into the assembly typically occurs immediately prior to board attachment.

High lead-end coplanarity in surface-mounted lead chip carriers is an important factor in reliable solder attachment to the printed board. Planarity may be measured from the lowest three leads of a leaded package. Coplanarity of 0.1 mm [0.004 in] maximum is recommended with 0.05 mm [0.002 in] preferred.

End terminations should be solder coated with a tin/lead alloy or a lead free equivalent. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a postplating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

For lead free finishes a combination of tin, silver and copper is the prevalent replacement for the tin/lead finish. Solderability testing should be applied per IPC-J-STD-002 to determine attachment capability of the applicable component type.

For marking, all parts shall be marked with a part number and "Pin 1" location. "Pin 1" location may be molded into the plastic body.

A carrier package format consisting of bulk rods, 24 mm tape/8-12 mm pitch is preferred for best handling. Tube carriers are also used.

Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215 °C [419 °F]. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260 °C [500 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

**12.1 PLCC** Plastic leaded chip carriers (PLCC) are employed where a hermetic seal is not required. Other constraints include limited temperature range (typically 0 °C [32 °F] or 70 °C [158 °F]) and nominal environmental protection. As with plastic DIPs, they have the advantage of low cost as compared to ceramic packages (see Figure 12-1).

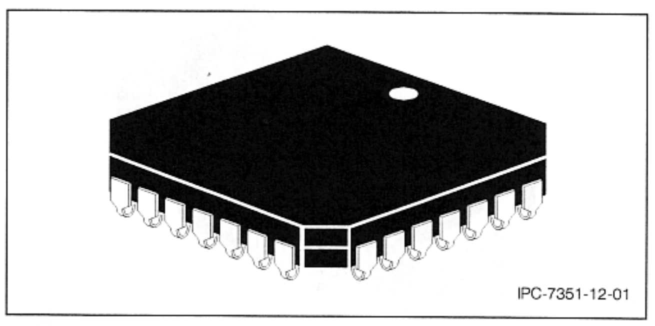



**Figure 12-1 PLCC Construction**

**12.1.1 Premolded Plastic Chip Carriers** The premolded plastic chip carrier was designed to be connected to the P&I substrate by means of a socket. Spring pressure on both sides of the package is intended to constrain movement as well as allow for substrate warpage as high as 0.5%. Solder attach to the P&I substrate is also possible. The design is also intended to make use of silicone encapsulant technology for chip coverage and protection.

**12.1.2 Postmolded Plastic Chip Carriers** The postmolded plastic leaded chip carrier is composed of a composite metal/dielectric assembly that includes a conductor lead frame and a molded insulating body. Compared to the premolded package which has an aperture for mounting microelectronic components, the postmolded package comes complete with no apertures. In both types of plastic chip carriers, all necessary plating operations are performed by the package manufacturer to eliminate tinning or plating by the user.

The Joint Device Engineering Council (JEDEC) defines the Type A Leaded Chip Carrier as a plastic package with leads wrapped down and around the body on all four sides. This package can be either directly mounted to a printed wiring board or used with a socket. It is available with 28, 44, 52, 68, 84, 100, or 124 leads. This family is based on 1.27 mm lead pitch. The original mechanical outline drawing of this package was defined based on a premolded package. However, actual construction is not specified and the package could be of postmolded construction.

Postmolded packages which have J-lead configurations and whose outlines are derived from outline MO-047 in JEDEC Publication are available in 20-, 28-, 44-, 52-, 68-, 84-, 100- and 124-lead counts with the same spacing.

**12.2 PLCCR** Plastic leaded chip carriers, rectangular (PLCCR) are employed where a hermetic seal is not required. Other constraints include limited temperature

range (typically 0 °C [32 °F] or 70 °C [158 °F]) and nominal environmental protection. As with plastic DIPs, they have the advantage of low cost as compared to ceramic packages (see Figure 12-2).

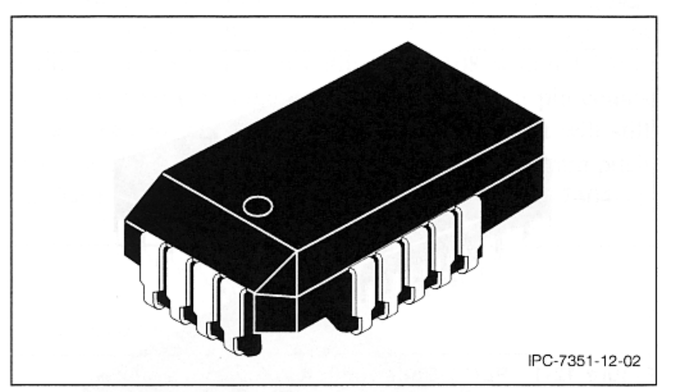



**Figure 12-2 PLCCR Construction**

**12.2.1 Premolded Plastic Chip Carriers** The premolded plastic chip carrier was designed to be connected to the P&I substrate by means of a socket. Spring pressure on both sides of the package is intended to constrain movement as well as allow for substrate warpage as high as 0.5%. Solder attach to the P&I substrate is also possible. The design is also intended to make use of silicone encapsulant technology for chip coverage and protection.

**12.2.2 Postmolded Plastic Chip Carriers** The postmolded plastic leaded chip carrier is composed of a composite metal/dielectric assembly that includes a conductor lead frame and a molded insulating body. Compared to the premolded package which has an aperture for mounting microelectronic components, the postmolded package comes complete with no apertures. In both types of plastic chip carriers, all necessary plating operations are performed by the package manufacturer to eliminate tinning or plating by the user.

The Joint Electron Device Engineering Council (JEDEC) defines the Type A Leaded Chip Carrier as a plastic package with leads wrapped down and around the body on all four sides. This package can be either directly mounted to a printed wiring board or used with a socket. It is available with 28, 44, 52, 68, 84, 100, or 124 leads. This family is based on 1.27 mm lead pitch. The original mechanical outline drawing of this package was defined based on a premolded package. However, actual construction is not specified and the package could be of postmolded construction.

Postmolded packages which have J-lead configurations and whose outlines are derived from outline MO-047 in JEDEC Publication are available in 20-, 28-, 44-, 52-, 68-, 84-, 100- and 124-lead counts with the same spacing.

## 13 IPC-7357 POST (DIP) LEADS, TWO SIDES

A method of modifying DIPs for surface mounting is the "I" mounting technique. This involves simply cutting the DIP leads to a short length and placing the device on a pattern of lands to be soldered along with the other surface mounted devices. Construction is usually made of plastic or ceramics (see Figure 13-1).

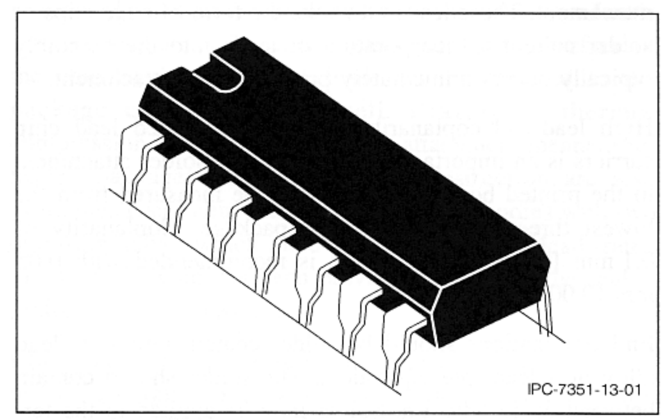



**Figure 13-1 DIP Construction**

**13.1 Termination Materials** End terminations should be solder coated with a tin/lead alloy or a lead free equivalent. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a postplating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

For lead free finishes a combination of tin, silver and copper is the prevalent replacement for the tin/lead finish. Solderability testing should be applied per IPC-J-STD-002 to determine attachment capability of the applicable component type.

**13.2 Marking** Parts shall be marked with the part number and a date code. In addition, pin 1 shall be identified.

**13.3 Carrier Package Format** Carrier format may be tubes or as agreed to between user and vendor.

**13.4 Resistance to Soldering** The parts should be capable of withstanding ten cycles through a standard reflow system operating at 215 °C [419 °F]. Each cycle shall consist of a minimum of 60 seconds exposure at 215T°C [419 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

## 14 IPC-7358 AREA ARRAY COMPONENTS (BGA, FBGA, CGA)

The area array device family includes square and rectangular package configurations and is furnished in a variety of base materials. This device family includes Ball Grid Array (BGA) parts (rigid, flexible or ceramic substrate); Fine Pitch Ball Grid Array (FBGA) parts (rigid or flexible substrate); and Column Grid Array (CGA) parts (ceramic substrates).

The area array device families are generally marked with the manufacturer's name or symbol, part number, date code and orientation mark in the corner near contact location A1.

Area array devices may be furnished in matrix tray or tape and reel packaging formats. Tape and reel packaging is generally preferred for high volume assembly. Plastic trays and reels must be transported and stored in moisture proof containers. When plastic array devices are exposed to the environment for an extended period of time, moisture may absorb into the device. The absorbed moisture, if excessive, may expand (when exposed to higher temperatures typical of reflow solder process), causing cracking and other physical damage.

Area array devices are typically attached to the host interface structure using eutectic solder alloy, however, optional methods of attachment may include electrically conductive epoxy or polymer. There is also a process difference between the solder application for those terminations that collapse slightly during soldering and those terminations that do not collapse where a significant amount of additional solder paste is required. Array package assembly should not require specialized equipment or processes beyond that used for vision assisted SMT pick and place.

In conjunction with the proper land size, the volume of solder paste application is a fundamental parameter to keep under control in order to have a good reflow quality yield and a reliable solder joint. Paste volume deposition may be a matter of SPC adoption at print process step.

**14.1 Area Array Configurations** For additional detail on package variations, mechanical feature dimensions and allowable physical tolerances beyond the following sectional descriptions, refer to the JEDEC Publication JEP95 and IPC-7095.

**14.1.1 BGA Packages** Figure 14-1 shows the elements of a BGA. JEDEC Publication JEP95, Section 4.14, defines a Ball Grid Array Package family. A Ball Grid Package (BGA) is a square or rectangular 1.50 mm, 1.27 mm, & 1.00 mm pitch package with an array of metallic balls or columns on the underside of the package. The main body of the package has a metallized circuit pattern applied to a dielectric structure. To this package body, the semiconductor die(s) is attached to either the top or bottom surface. On the underside of the dielectric is an array pattern of metallized balls/columns which form the mechanical and electrical connection from the package body to a mating feature such as a printed circuit board. The array contact material will allow conventional reflow solder or other attachment processes. The surface that contains the die may be encapsulated by various techniques to protect the semiconductor. Figure 14-2 compares the top surface attached die to the cavity down configuration.

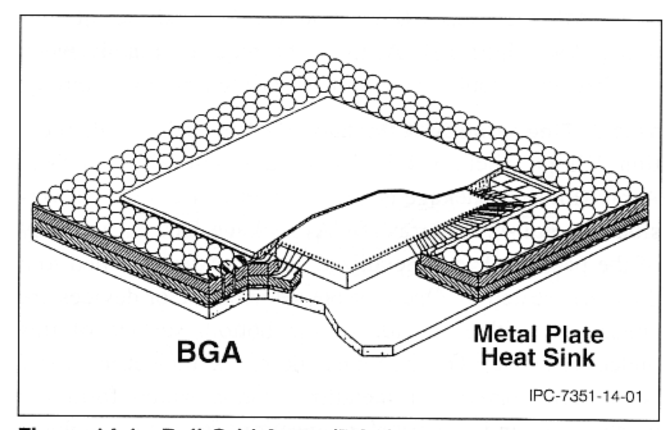



**Figure 14-1 Ball Grid Array (BGA) IC Package Example**

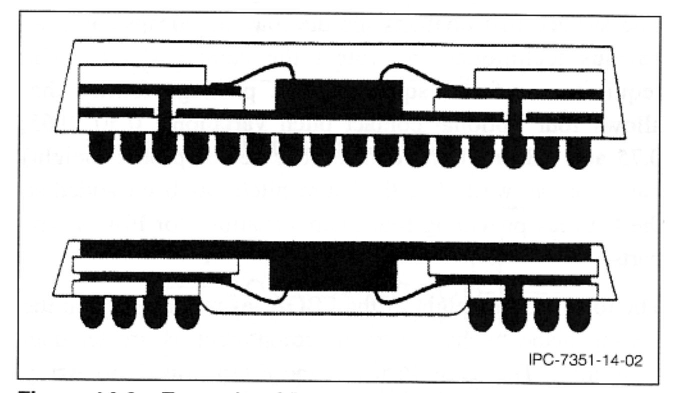



**Figure 14-2 Example of Plastic BGA Package Configurations**

**14.1.1.1 Termination Materials** The BGA ball termination may consist of a variety of metal alloys. Some of these include balls with some lead content such as 37Pb63Sn, 90Pb10Sn, 95Pb5Sn, while others do not contain lead such as Sn96.5Ag3.0Cu0.5, Sn96.5Ag3.5, Sn-9Zn-0.003Al. It is a good recommendation to use the same alloy, in a paste form, to attach the BGA balls to the mounting substrate; however some of the balls that do not collapse require a paste that is more conducive to reflow temperatures.

For lead free finishes a combination of tin, silver and copper is the prevalent replacement for the tin/lead finish. Solderability testing should be applied per IPC-J-STD-002 to determine attachment capability of the applicable component type.

**14.1.1.2 Process Considerations** BGAs are usually processed using standard reflow solder processes. Parts should be capable of withstanding three cycles through a

standard reflow system operating within a range of 235 °C to 260 °C [455 °F to 500 °F] depending on the attachment alloy being used. Each cycle shall consist of 60 to 90 seconds exposure at the particular temperature selected. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

It is important to consider that Plastic BGAs are moisture sensitive device/components (MSD). Precaution must be taken during the printed board assembly process in order to avoid MSD damages (Delamination, Cracks, etc). Traceability for baking PBGA, might be required mainly when attached in a double sided/reflow printed board assembly.

**14.1.2 Fine Pitch BGA Package (FBGA)** JEDEC Publication JEP95, Section 4.5, defines a Fine-pitch Ball Grid Array (FBGA) package is a reduced-pitch (<1.00 mm) version of a Ball-Grid-Array (BGA) package. The carrier body of the package has a metallized circuit pattern applied to a dielectric structure. One or more semiconductor devices are attached to either the top or the bottom surface of this dielectric carrier. On the underside of the dielectric carrier is an array pattern of metallized balls, which form the mechanical and electrical connection from the package body to a mating feature such as a printed circuit board. The surface that contains the die may be encapsulated by various techniques to protect the semiconductor. The requirements for a square FBGA package family that allows four optional contact pitch variations; 0.50, 0.65, 0.75 and 0.80 mm and defines four device profile (height) variations as well. The 0.75 mm pitch has been added to the list thus providing four pitch variations for FBGA type parts.

The total profile height of the FBGA, as measured from the seating plane to the top of the component, is greater than 1.70 mm. The Low-Profile Fine-Pitch Ball-Grid-Array (LFBGA) and is a *reduced-height* version of an FBGA. The total profile height of the LFBGA as measured from the seating plane to the top of the component, is no greater than 1.20 mm. Thin-Profile Fine-Pitch Ball-Grid-Array (TFBGA) is a *reduced-height* version of an FBGA with a total profile height as measured from the seating plane to the top of the component that does not exceed 1.00 mm and the Very-Thin-Profile Fine-Pitch Ball-Grid-Array (VFBGA) is a *reduced-height* version of an FBGA with a total profile height as measured from the seating plane to the top of the component that is at or below 0.80 mm.

The JEDEC design guide for FBGA allows the manufacturer the option to increase ball diameter as the spacing or pitch between ball contact centers increase as compared in Table 14-1. As of this release JEDEC standards do not support the 0.75 mm pitch, however the industry has some parts available in that pitch.

The larger ball diameter option has been allowed to accommodate packages using rigid interposer structures. The larger diameter ball may compensate to a degree, for the wide mismatch of the coefficient of thermal expansion (CTE) between the silicon die and the rigid PCB structure.

**Table 14-1 JEDEC Standard JEP95 Allowable Ball Diameter Variations for FBGA (mm)**

| | Ball Diameter | | |
|---|---|---|---|
| Ball Pitch | Minimum | Nominal | Maximum |
| 0.80 | 0.45 | 0.50 | 0.55 |
| 0.80 | 0.35 | 0.40 | 0.45 |
| 0.80 | 0.25 | 0.30 | 0.35 |
| 0.65 | 0.35 | 0.40 | 0.45 |
| 0.65 | 0.25 | 0.30 | 0.35 |
| 0.50 | 0.25 | 0.30 | 0.35 |

Fine pitch ball parts may require special processing outside the normal pick/place and reflow manufacturing operations. This requirement relates to the amount of solder paste, the precision of the placement machine and the soldering process profile, to permit all parts to become attached at the same time that the FBGA is reflowed.

Ball termination and process considerations for FBGA are the same as that for BGA as described in 14.1.1.1 and 14.1.1.2.

**14.1.3 Ceramic Column Grid Arrays (CGA)** Solder column contacts typical of that illustrated in Figure 14-3 are used for larger ceramic-based packages (32.0 mm to 45.0 mm). The package resembles the earlier pin-grid-array but with closer contact pitch and more fragile leads (columns). The column contact diameter is approximately 0.5 mm with its length varying from 1.25 mm to 2.0 mm. The columns are attached to the package either by eutectic (Sn63Pb37) solder or they are cast in place using 90% Pb and 10% Sn.

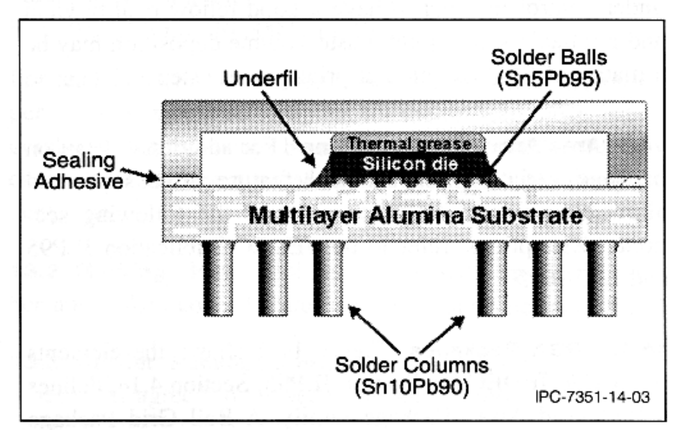



**Figure 14-3 Ceramic Column Grid Array (CGA) Package (Cross-Sectional View)**

The longer columns typically increase solder joint reliability by absorbing a great deal of the stresses created by the CTE mismatch between the ceramic package and the board. Longer columns, on the other-hand, may reduce

electrical performance and will increase the overall package profile. Also the columns are not as rugged as ball contact and are susceptible to handling damage.

**14.2 General Configuration Issues**

**14.2.1 Device Outlines** The Grid Array package outlines detailed in this document are furnished in JEDEC Publication JEP95. The overall outline specification for the array device allows a great deal of flexibility as far as lead pitch, contact matrix pattern and construction. The JEDEC standards allow for die attachment on either side of the interface structure (cavity up or cavity down). Refer to IPC-7096 for further definition and interconnect schemes for BGAs. The example shown in Figure 14-4 illustrates two 225 I/O devices with a common package outline but, with the variation of contact pitch, a unique matrix format is provided.

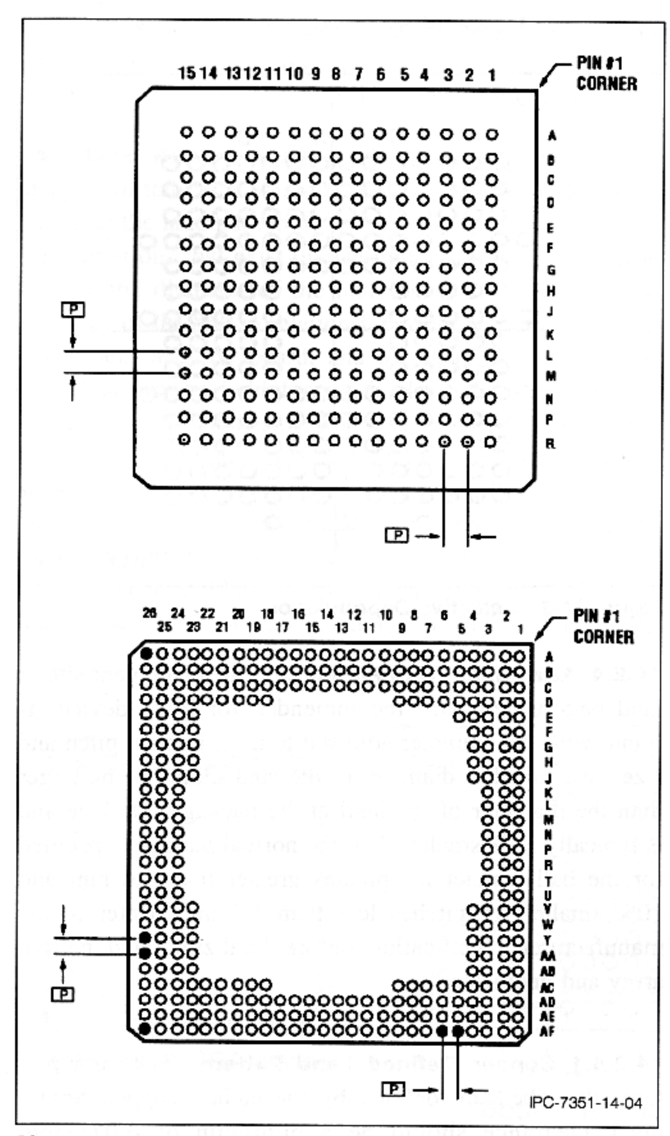



**Figure 14-4 Bottom View of BGA Devices**

**14.2.2 Contact Matrix Options** Contacts may be distributed in a uniform pattern, however the matrix is always centered about the centerline of the package (see Figure 14-5). Contact depopulation is permitted at the discretion of the device manufacturer. Contact patterns can usually be described in the following methods: full even matrix, full odd matrix, perimeter matrix, or staggered matrix.

**14.2.2.1 Full Matrix** For a given package size, there are two full matrix possibilities: even and odd. One of them is the largest matrix that theoretically could fit on the package, given the size and pitch of the contacts. The other matrix is smaller by one row and column (see Figure 14-5).

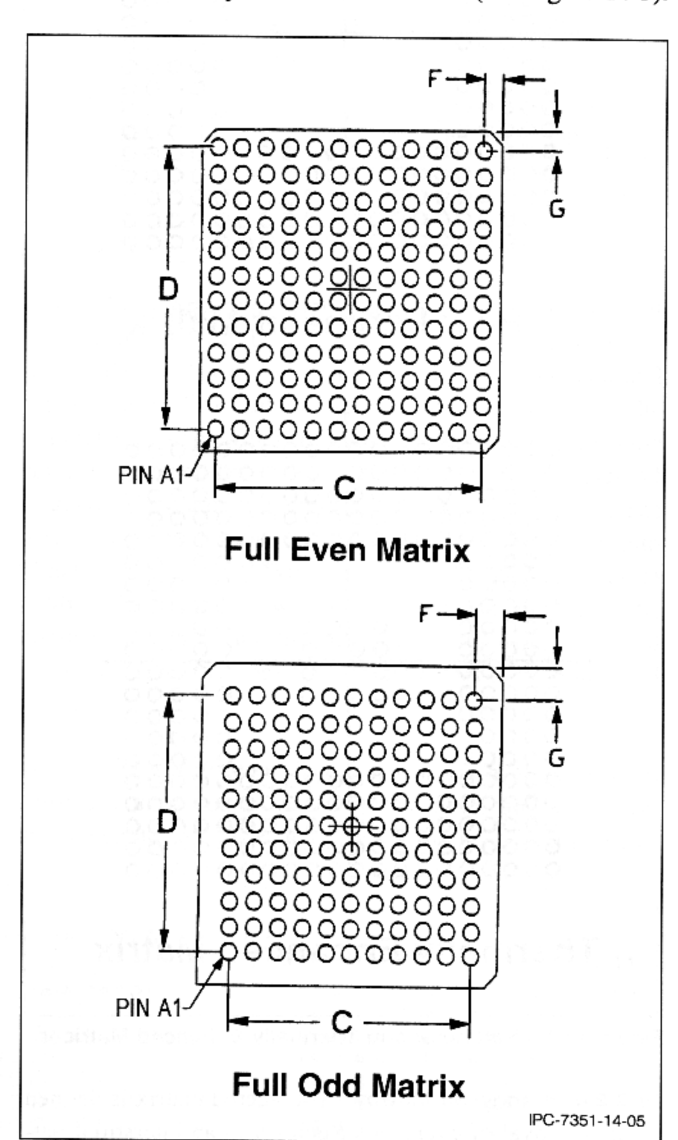



**Figure 14-5 One Package Size, Two Full Matrices**

**14.2.2.2 Perimeter Matrix** A perimeter matrix is achieved by removing an array of contacts from the center of the matrix. Center-depopulation does not affect the centerline of the matrix (see Figure 14-6). In addition, Perimeter matrices are usually described by the number of contact perimeters.

**14.2.2.3 Thermally Enhanced Matrix** A thermally enhanced matrix is a perimeter matrix with contacts added back in the center (see Figure 14-6).

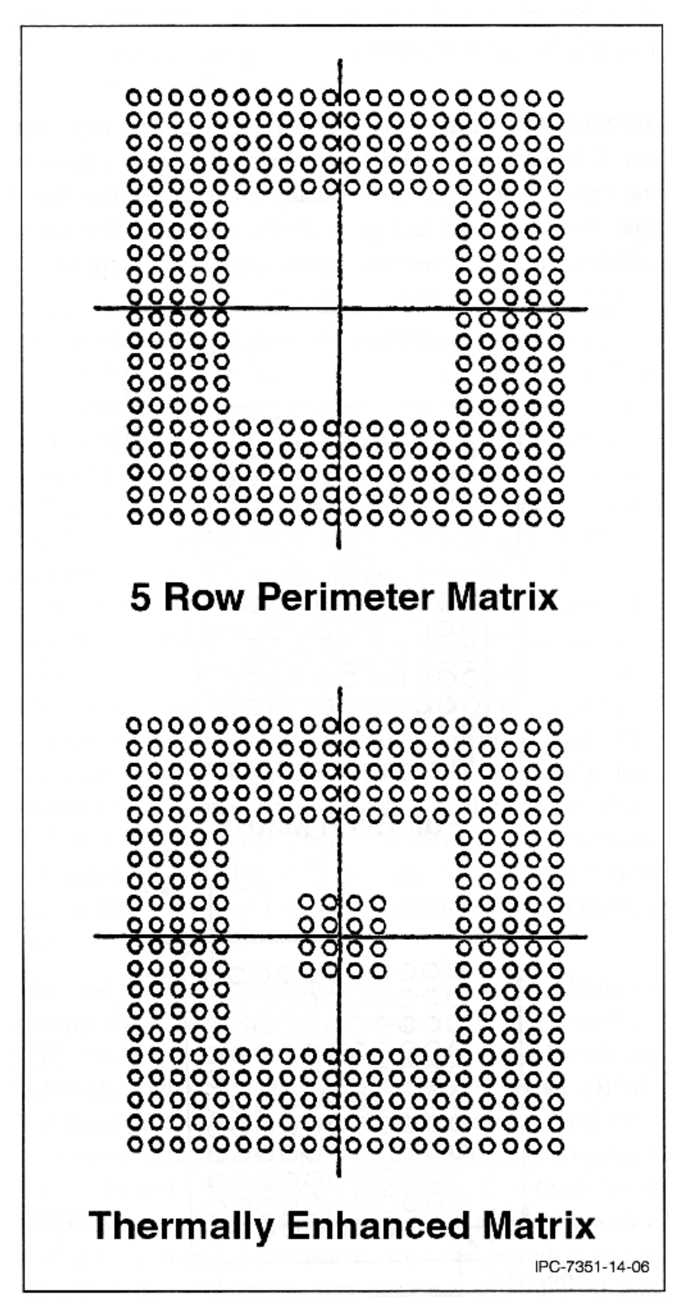



Figure 14-6 Perimeter and Thermally Enhanced Matrices

**14.2.2.4 Staggered Matrix** A staggered matrix is defined by the removal of every other contact in an interstitial pattern. This provides an effective minimum center-to-center contact spacing of $\sqrt{2}$ x pitch of the full matrix (see Figure 14-7). In order to retain the A1 contact position, the staggered matrix must be developed using a full odd matrix.

**14.2.3 Selective Depopulation** In addition to depopulation methods which lead to the matrices described above, contacts may be removed selectively. Selective depopulation can be accomplished in any manner as long as the pattern matrix is not shifted from the center of the package outline (see Figure 14-8).

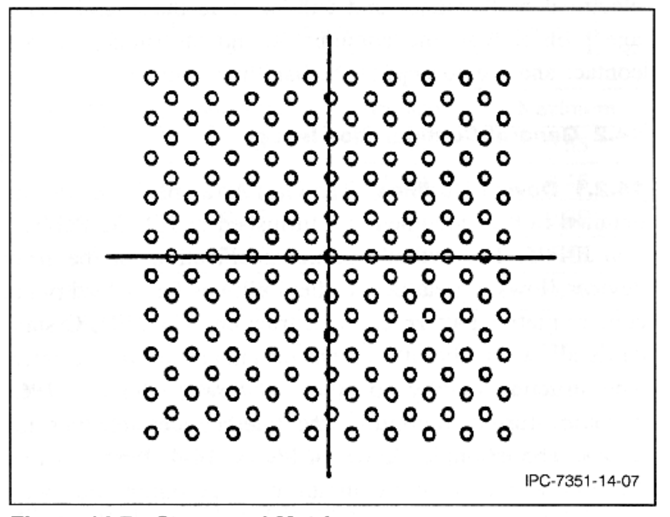



Figure 14-7 Staggered Matrix

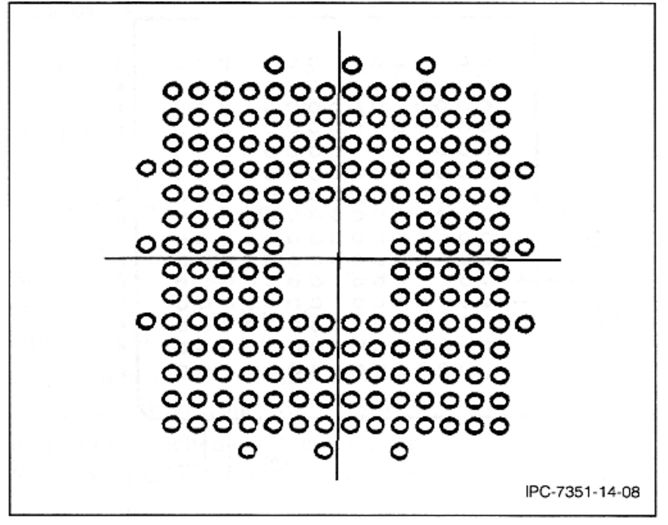



Figure 14-8 Selective Depopulation

**14.2.4 Attachment Site Planning** The attachment site or land pattern geometry recommended for BGA devices is round with the diameter adjusted to meet contact pitch and size variation. The diameter of the land should be no larger than the diameter of the land at the package interface and is typically 20% smaller than the normal diameter specified for the ball contact for pitches greater than 1.0 mm and 10% smaller for pitches less than 1.0 mm. Refer to the manufacturer specification before finalizing land pattern array and geometry.

**14.2.4.1 Copper Defined Land Pattern** The land patterns described are defined by the etched copper. Solder mask clearance should be a minimum of 0.075 mm [0.00295 in] from the etched copper land. For applications requiring a clearance that is less than recommended, consult with the printed board supplier.

**14.2.4.2 Solder Mask Defined Land Pattern** If solder mask defined patterns are used, then adjust land pattern diameter accordingly (see 14.4).

**14.2.5 Defining Contact Assignment** Array contact identification is assigned by the column and row location. For example, A1 contact position is always at an outside corner position with alpha characters arranged in a vertical (row) pattern from top to bottom. Numeric characters are assigned in a horizontal (column) axis (I, O, Q, S, X and Z are omitted) (see Figure 14-9).

The designer should note that the A1 position is at the upper left hand corner when the device is viewed from the top. Contact pattern is defined when viewed from the bottom. The land pattern provided on the host substrate is opposite of the contact pattern (with A1 contact position again at the upper left).

**14.3 Handling and Shipping** For information on trays and shipping containers refer to ACH:EIA-481-A, ACH:EIA-481-3, JEDEC CO-028, and JEDEC CO-029.

**14.4 Land Pattern Analysis** The following provides an analysis of tolerance assumptions and result in solder joints based on the land pattern dimensions shown in Figure 14-9. The variations that exist in determining these land patterns include the diameter of the individual ball, the positional accuracy of the ball in relationship to a true position on the component and the board, and the manufacturing allowance that can be held for the land on the substrate that mounts the particular ball. The land pattern of the component (where the ball is attached) and the land pattern of the substrate mounting structure (printed board) should be as similar as possible. Component manufacturers have made their determinations that the land pattern of pad on the component should be less than the ball diameter. They base their conclusions on the resulting nominal ball diameter with a slight reduction in the land approximation. Pitch plays a large role in the determination of what ball diameters can be used in various combinations. Table 14-2 shows the characteristics of those balls that are used with pitches of 1.5 mm through 1.0 mm, as well as future ball sizes whose pitches fall between 0.40 mm and 0.25 mm.

**Table 14-2 Ball Diameter Sizes (mm)**

| Nominal Ball Diameter | Total Variation | Pitch |
|---|---|---|
| 0.75 | 0.90 - 0.65 | 1.5, 1.27 |
| 0.60 | 0.70 - 0.50 | 1.0 |
| 0.50 | 0.55 - 0.45 | 1.0, 0.80 |
| 0.45 | 0.50 - 0.40 | 1.0, 0.80, 0.75 |
| 0.40 | 0.45 - 0.35 | 0.80, 0.75, 0.65 |
| 0.30 | 0.35 - 0.25 | 0.80, 0.75, 0.65, 0.50 |
| 0.25 | 0.28 - 0.22 | 0.40 |
| 0.20 | 0.22 - 0.18 | 0.30 |
| 0.15 | 0.17 - 0.13 | 0.25 |

**14.4.1 Land Approximation** In each instance, component manufacturers and board designers are encouraged to reduce the land size by some percentage of the nominal ball diameter. The amount of reduction is based on the original ball size, which is used to determine the average land. In determining the relationship between nominal characteristics, a manufacturing allowance for land size has been determined to be 0.1 mm between the Maximum Material Condition (MMC) and Least Material Condition (LMC). Table 14-3 shows the reduction characteristics, the nominal land size, and the target land dimensions, as well as future approximations for ball diameters of 0.25 mm and below.

**14.4.2 Total Variation** The total variation of the system considers three major issues: positioning, ball tolerance, and substrate tolerance. All three attributes added together

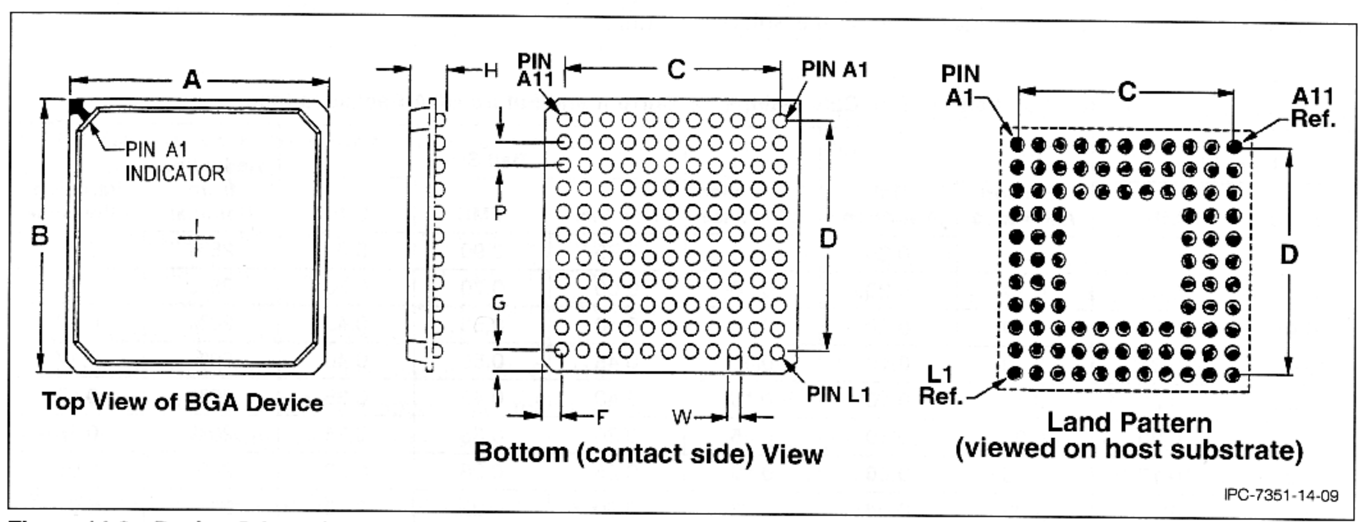



**Figure 14-9 Device Orientation and Contact A1 Position**

**Table 14-3 Land Approximation (mm)**

| Nominal Ball Diameter | Reduction | Nominal Land Diameter | Land Variation |
|---|---|---|---|
| 0.75 | 25% | 0.55 | 0.60 - 0.50 |
| 0.60 | 25% | 0.45 | 0.50 - 0.40 |
| 0.50 | 20% | 0.40 | 0.45 - 0.35 |
| 0.45 | 20% | 0.35 | 0.40 - 0.30 |
| 0.40 | 20% | 0.30 | 0.35 - 0.25 |
| 0.30 | 20% | 0.25 | 0.25 - 0.20 |
| 0.25 | 20% | 0.20 | 0.20 - 0.17 |
| 0.20 | 20% | 0.15 | 0.15 - 0.12 |
| 0.15 | 20% | 0.10 | 0.10 - 0.08 |

result in a worst case analysis, however as with other land patterns in the standard, a statistical average is determined by using the RMS (root, mean, square) value. Table 14-4 shows the total variation in the system for each of the four ball sizes identified in the standard.

**Table 14-4 BGA Variation Attributes (mm)**

| Nominal Ball Size | Positional Allowance | Ball Tolerance | Substrate Tolerance | Variation RMS Value |
|---|---|---|---|---|
| 0.75 | 0.1 dia. DTP | 0.25 | 0.10 | 0.25 |
| 0.60 | 0.1 dia. DTP | 0.20 | 0.10 | 0.24 |
| 0.50 | 0.1 dia. DTP | 0.10 | 0.10 | 0.17 |
| 0.45 | 0.1 dia. DTP | 0.10 | 0.10 | 0.17 |

It should be noted that the target value for lands on the substrate of the component or the board should be at Maximum Material Condition. The variation from the Maximum Material Condition indicates that ball-to-land misalignment is achieved by taking the maximum land size and subtracting the variation. The resulting dimension would indicate the amount of attachment area that would result from a system where all conditions are at a negative instance. For lands that are solder mask-defined, the land size should be increased by the amount of encroachment of the solder mask. As an example, if the requirement is that solder mask should be on the land by 0.05 mm, then the maximum land size should be increased by 0.1 mm. It should be noted that for solder mask-defined lands, since the land size increases, the opportunity to route conductors between lands is impacted by reducing the available area for conductor width and spacing.

**14.4.3 Future Ball Conditions** Although not required for the BGAs shown in the present release of IPC-7351, projected future ball sizes of 0.40 mm pitch and below are shown in Table 14-2. Their projected land size approximations for ball diameters of 0.25 mm and below are shown in Table 14-3.

**14.4.4 Land Pattern Calculator** The land pattern calculations for BGAs are based on ball size. As a result of ball variation and component conditions, Table 14-5 shows the land pattern calculator headings needed to describe the variations in the system. This data is usually described at the Maximum Material Condition for nonsolder mask-defined lands and is dimension "X" in the IPC-7351 datasheets for BGA land patterns.

## 15 IPC-7359 NO LEAD COMPONENTS (QFN, SON, LCC)

**15.1 LCC** A leadless chip carrier is a ceramic package with integral surface-metallized terminations. Leadless Types A, B, and D chip carriers have a chamfered index corner that is larger than that of Type C. Another difference between the A, B, and D types and Type C is the feature in the other three corners. The types A, B, and D, were designed for socket applications and printed wiring interconnections. The Type C is primarily intended for direct attachment through reflow soldering. This application difference is the main reason for their mechanical differences. These packages mount in different orientations, depending on type, mounting structure and preferred thermal orientation.

**Table 14-5 Land-to-Ball Calculations for Current and Future BGA Packages (mm)**

| Land Size | | Location Allowance | Ball Variation | PCB Fabrication Allowance | Ball Size | | | % Reduction from Nominal | Variation Allowance |
|---|---|---|---|---|---|---|---|---|---|
| MMC | LMC | | | | Nominal | MMC | LMC | | |
| 0.60 | 0.50 | 0.10 | 0.25 | 0.10 | 0.75 | 0.90 | 0.65 | 25% | 0.25 |
| 0.50 | 0.40 | 0.10 | 0.20 | 0.10 | 0.60 | 0.70 | 0.50 | 25% | 0.20 |
| 0.45 | 0.35 | 0.10 | 0.10 | 0.10 | 0.50 | 0.55 | 0.45 | 20% | 0.17 |
| 0.40 | 0.30 | 0.10 | 0.10 | 0.10 | 0.45 | 0.50 | 0.40 | 20% | 0.17 |
| 0.35 | 0.25 | 0.10 | 0.10 | 0.10 | 0.40 | 0.45 | 0.35 | 20% | 0.17 |
| 0.25 | 0.20 | 0.05 | 0.10 | 0.05 | 0.30 | 0.35 | 0.25 | 20% | 0.15 |
| 0.20 | 0.17 | 0.05 | 0.06 | 0.03 | 0.25 | 0.28 | 0.22 | 20% | 0.08 |
| 0.15 | 0.12 | 0.05 | 0.04 | 0.03 | 0.20 | 0.22 | 0.18 | 20% | 0.07 |
| 0.10 | 0.08 | 0.05 | 0.04 | 0.02 | 0.17 | 0.17 | 0.13 | 20% | 0.07 |

Leadless Type A is intended for lid-down mounting in a socket, which places the primary heat-dissipating surface away from the mounting surface for more effective cooling in air-cooled systems.

Type C is a ceramic package similar to leadless Type B except for corner configuration. The 1.27 mm center family, which includes both leadless and leaded devices, is designed to mount on a common mounting pattern. They may be directly attached to the mounting structure, or can be plugged into sockets. One basic restriction is that there shall be no terminals in the corners of the package. There are a number of common sizes.

End terminations should be solder coated with a tin/lead alloy or a lead free equivalent. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a postplating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

For lead free finishes a combination of tin, silver and copper is the prevalent replacement for the tin/lead finish. Solderability testing should be applied per IPC/EIA-J-STD-001 to determine attachment capability of the applicable component type.

**15.1.1 Marking** All parts shall be marked with a part number and "Pin 1" location. "Pin 1" location may be molded into the plastic body.

**15.1.2 Carrier Package Format** Tube carriers are preferred for best handling.

**15.1.3 Process Considerations** LCCs are usually processed using standard solder reflow processes. Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215° C [419 °F]. Each cycle shall consist of 60 seconds exposure at 215° C [419 °F]. See IPC/JEDEC J-STD-020 for appropriate reflow cycles and profiles when using lead free solders.

**15.2 Quad Flat No-Lead (QFN)** The Quad Flat No-Lead (QFN) package is a near CSP plastic encapsulated package with a copper leadframe substrate. This is a leadless package where electrical contact to the PCB is made by soldering the lands on the bottom surface of the package to the PCB, instead of the conventional formed perimeter leads. The exposed die attach paddle on the bottom efficiently conducts heat to the PCB and provides a stable ground through down bonds or electrical connections through conductive die attach material. The design of the QFN package also allows for flexibility. Its enhanced electrical performance enables the standard 2 GHz frequency to be increased up to 10 GHz with some design considerations (see Figures 15-1 and 15-2).

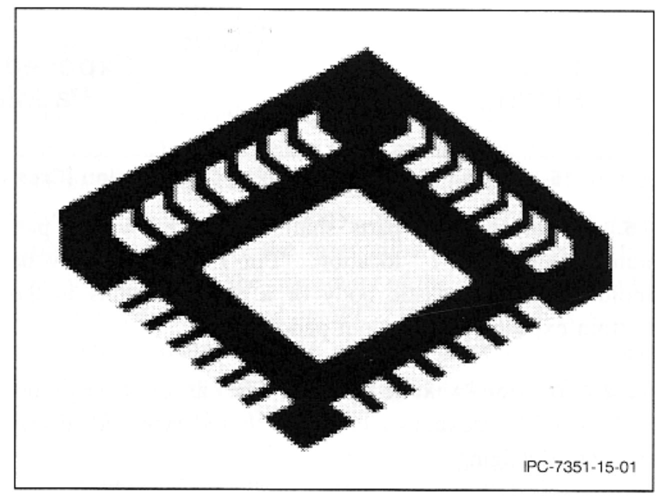



**Figure 15-1 Quad Flat No-Lead (QFN) Construction**

Solderable areas of the mating surfaces on the end terminations (package bottom side) should be solder coated with a tin/lead alloy or a lead free equivalent. Ends/sides of the terminals are not designed as a solderable surface and are not required to be plated, as this is a physical impossibility with many current manufacturing processes. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a postplating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

For lead free finishes a combination of tin, silver and copper is the prevalent replacement for the tin/lead finish. Solderability testing should be applied per IPC-J-STD-002 to determine attachment capability of the applicable component type.

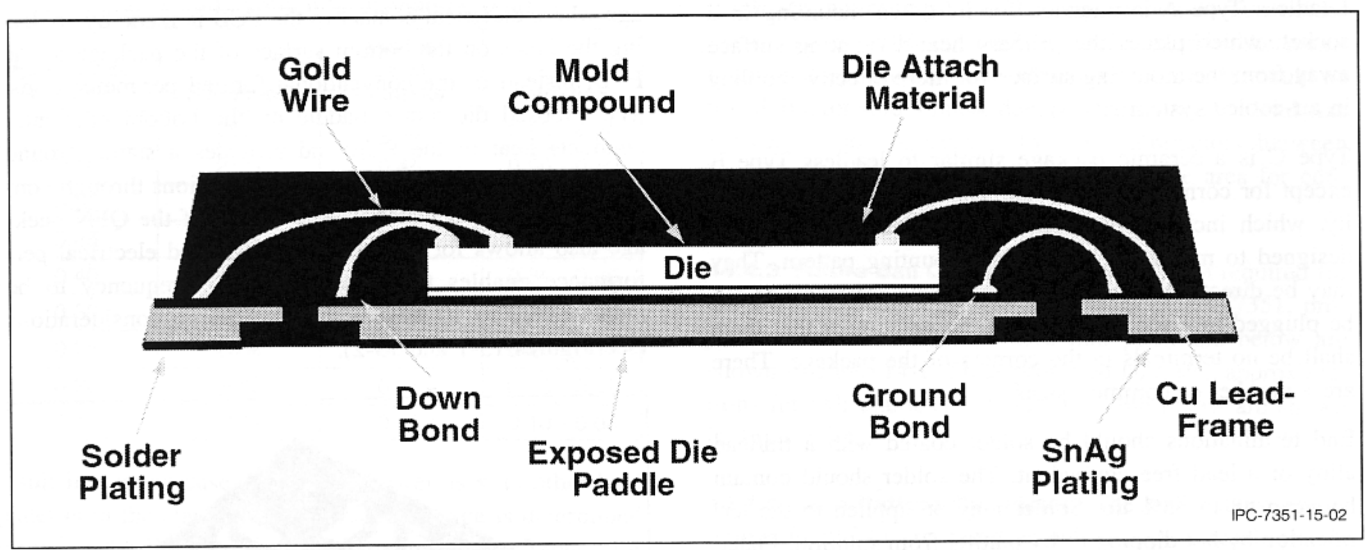



**Figure 15-2 Quad Flat No-Lead (QFN) Construction (Cross-Sectional View)**

**15.2.1 Marking** All parts shall be marked with a part number and "Pin 1" location. "Pin 1" location may be molded into the plastic body or a chamfer/radius in the bottom exposed pad (bottom paddle).

**15.2.2 Carrier Package Format** The carrier package format for QFN packages include embossed tape and reel as well as packaging trays.

**15.2.3 Process Considerations** Because of the small lead surface area and the sole reliance on printed solder paste on the PCB surface, the formation of reliable solder joints for the QFN package can be a challenge. This is further complicated by the large thermal pad underneath the package and its proximity to the inner edges of the leads. Special considerations are needed in stencil design and paste printing for both perimeter and thermal pads. Since surface mount process varies from company to company, careful process development is recommended.

The optimum and reliable solder joints on the perimeter pads should have about 50 µm to 75 µm standoff height. A side fillet is not required since the sides are not designed as a solderable surface (see IPC-A-610).

**15.2.4 Solder Resist Considerations** The solder resist opening should be 120 µm to 150 µm larger than the land size resulting in 60 µm to 75 µm clearance between the copper land and solder resist. This allows for solder resist registration tolerances, which are typically between 50 µm to 65 µm, depending upon the board fabricators' capabilities. Typically each land on the PCB should have its own solder resist opening with a web of solder resist between two adjacent lands. Since the web has to be at least 75 µm in width for the solder resist to adhere to the PCB surface, each land can have its own solder resist opening for lead pitch of 0.5 mm or higher, based on the land width dimensions. However, for 0.4 mm pitch parts with PCB land width of 0.25 mm, not enough space is available for solder resist web in between the land. In such cases, it is recommended to use the "gang" type solder resist opening shown in Figure 3-22 where a big opening is designed around all land on each side of the package with no solder resist in between the land.

**15.3 Small Outline No-Lead (SON)** The Small Outline No-lead Package (SON) is a rectangular semiconductor package with metal terminals along two sides of the bottom of the package. The terminals are either flush with the bottom or protruding slightly below the bottom of the package, with plastic mold compound present on three sides of each contact. The main body of the component is generally a molded plastic. The SON package is similar to the leaded SOIC family, though consuming less of the PCB area in comparison with the leaded SOIC. The part is a "leadless" package design with bottom paddle which can be soldered to the PCB. See Figure 15-3 for an example of a SON component.

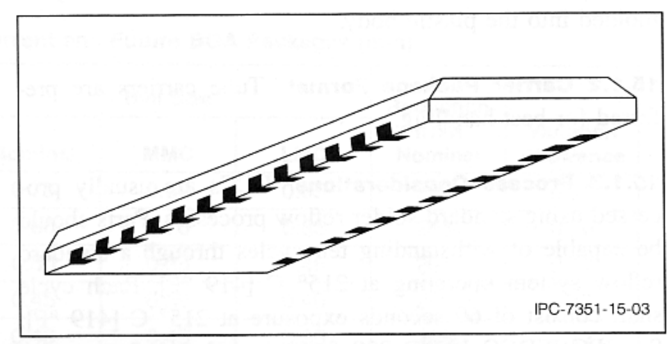



**Figure 15-3 Small Outline No-Lead (SON) Construction**

**15.3.1 Marking** All parts shall be marked with a part number and "Pin 1" location. "Pin 1" location may be molded into the plastic body or a chamfer/radius in the bottom exposed pad (bottom paddle).

**15.3.2 Carrier Package Format** The carrier package format for the SON includes anti-static tubes, since the units have no leads that can bend, as well as conductive carrier tape and reel.

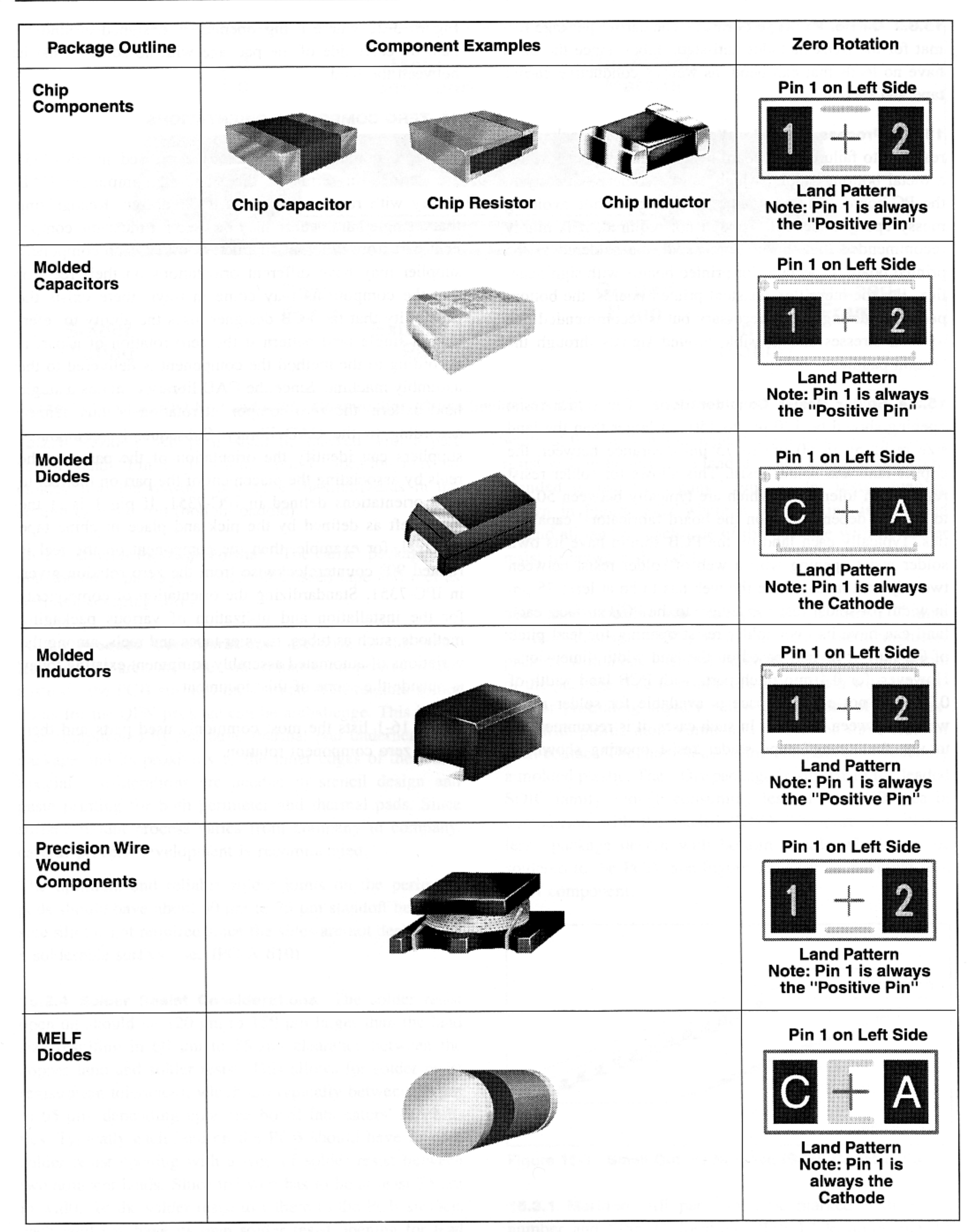
**15.3.3 Process Considerations** The SON package is resistant to failure from board bending (flexing); it features a metal bottom paddle, which can be soldered directly to the PC board. This adds adhesive strength while avoiding messy epoxy under-fill. Though not required, it is highly recommended that this bottom paddle be soldered to the printed board, especially for printed boards with significant flex. For the more flex-resistent printed boards, the bottom paddle soldering is not necessary but is recommended due to CTE stresses and possible ground signals through the bottom paddle.

**15.3.4 Solder Resist Considerations** The solder resist opening should be 120 µm to 150 µm larger than the land size resulting in 60 µm to 75 µm clearance between the copper land and solder resist. This allows for solder resist registration tolerances, which are typically between 50 µm to 65 µm, depending upon the board fabricators' capabilities. Typically each land on the PCB should have its own solder resist opening with a web of solder resist between two adjacent lands. Since the web has to be at least 75 µm in width for solder resist to adhere to the PCB surface, each land can have its own solder resist opening for lead pitch of 0.5 mm or higher, based on the land width dimensions. However, for 0.4 mm pitch parts with PCB land width of 0.25 mm, not enough space is available for solder resist web in between the land. In such cases, it is recommended to use the "gang" type solder resist opening shown in Figure 3-22 where a big opening is designed around all land on each side of the package with no solder resist in between the land.

## 16 ZERO COMPONENT ORIENTATIONS

The zero component orientations expressed in IPC-7351 are defined in terms of the standard component CAD library with respect to a given PCB design. Recognizing that a single land pattern may be used for the same component part from different suppliers and that each component supplier may have different orientations on their reels or that the components may come in trays, there exists the possibility that the PCB designer loses the ability to reference a single land pattern if the zero rotation of a part is according to the method the component is delivered to the assembly machine. Since the CAD library contains a single land pattern, the zero component rotation is thus defined according to the CAD library. Subsequently, component suppliers can identify the orientation of the parts on the reels by associating the placement of the part on the reel to zero orientations defined in IPC-7351. If pin 1 is at the lower left as defined by the pick and place machine tape and reel, for example, then the component on the reel is rotated 90° counterclockwise from the zero rotation given in IPC-7351. Standardizing the orientation of components for the installation and utilization of various packaging methods, such as tubes, trays or tapes and reels, among the variations of automated assembly equipment existing today is outside the scope of this document.

Figure 16-1 lists the most commonly used parts and their proper zero component rotation.



| Package Outline | Component Examples | Zero Rotation |
|---|---|---|
| Chip Components | Chip Capacitor, Chip Resistor, Chip Inductor | Pin 1 on Left Side<br>1 + 2<br>Land Pattern<br>Note: Pin 1 is always the "Positive Pin" |
| Molded Capacitors | | Pin 1 on Left Side<br>1 + 2<br>Land Pattern<br>Note: Pin 1 is always the "Positive Pin" |
| Molded Diodes | | Pin 1 on Left Side<br>C + A<br>Land Pattern<br>Note: Pin 1 is always the Cathode |
| Molded Inductors | | Pin 1 on Left Side<br>1 + 2<br>Land Pattern<br>Note: Pin 1 is always the "Positive Pin" |
| Precision Wire Wound Components | | Pin 1 on Left Side<br>1 + 2<br>Land Pattern<br>Note: Pin 1 is always the "Positive Pin" |
| MELF Diodes | | Pin 1 on Left Side<br>C + A<br>Land Pattern<br>Note: Pin 1 is always the Cathode |

**Figure 16-1 Zero Component Rotations for Common Package Outlines**

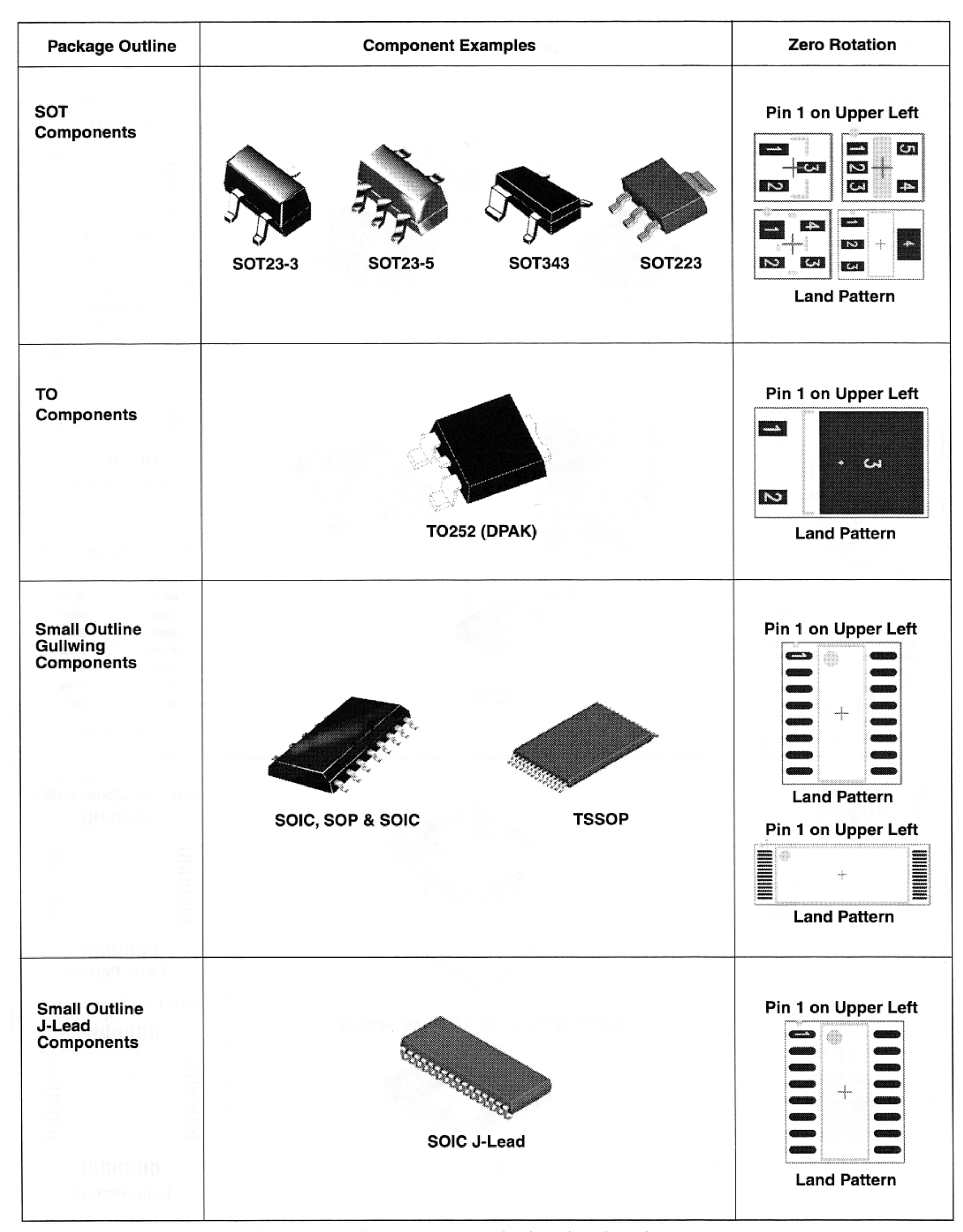



**Figure 16-1 Zero Component Rotations for Common Package Outlines (continued)**

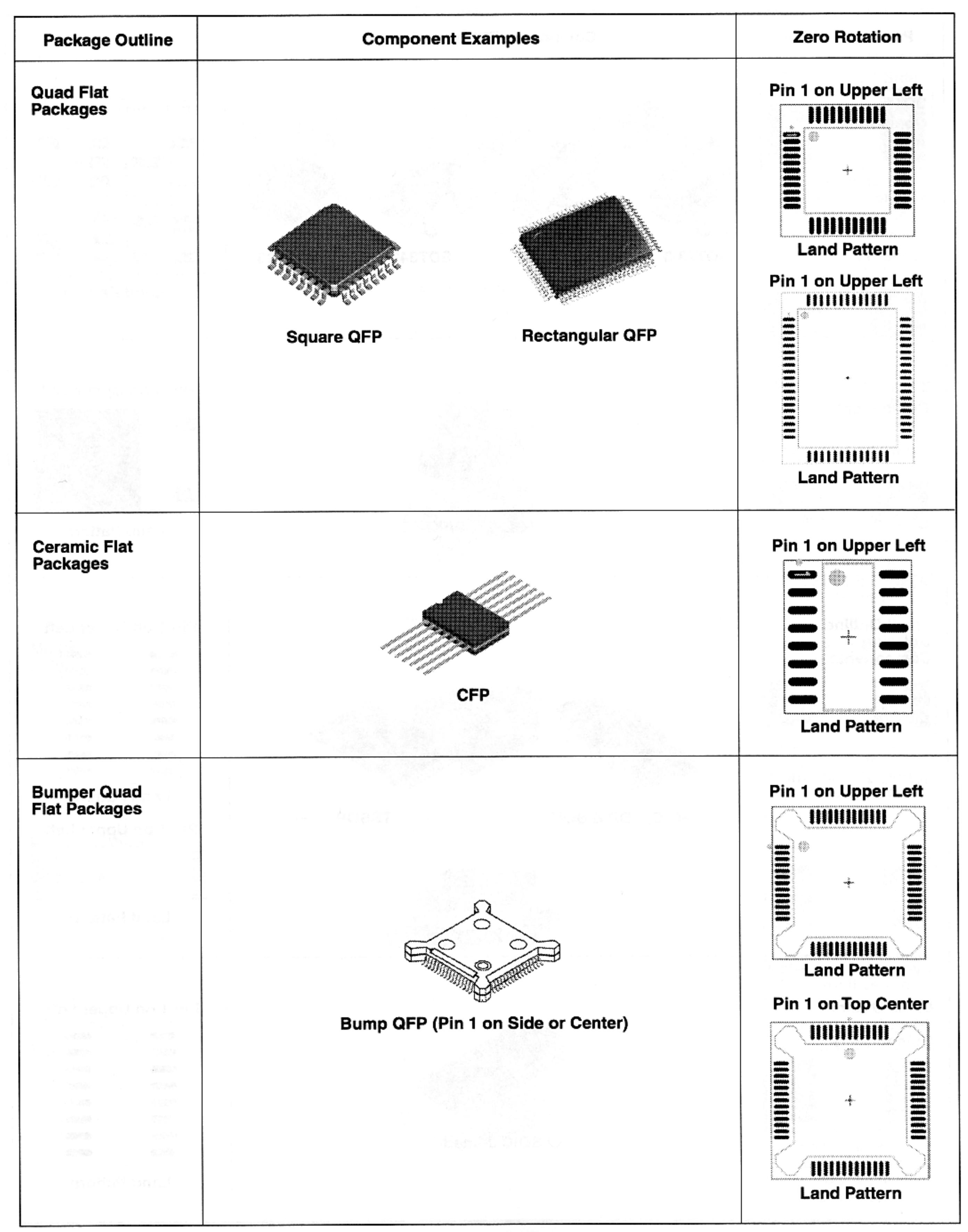



**Figure 16-1 Zero Component Rotations for Common Package Outlines (continued)**

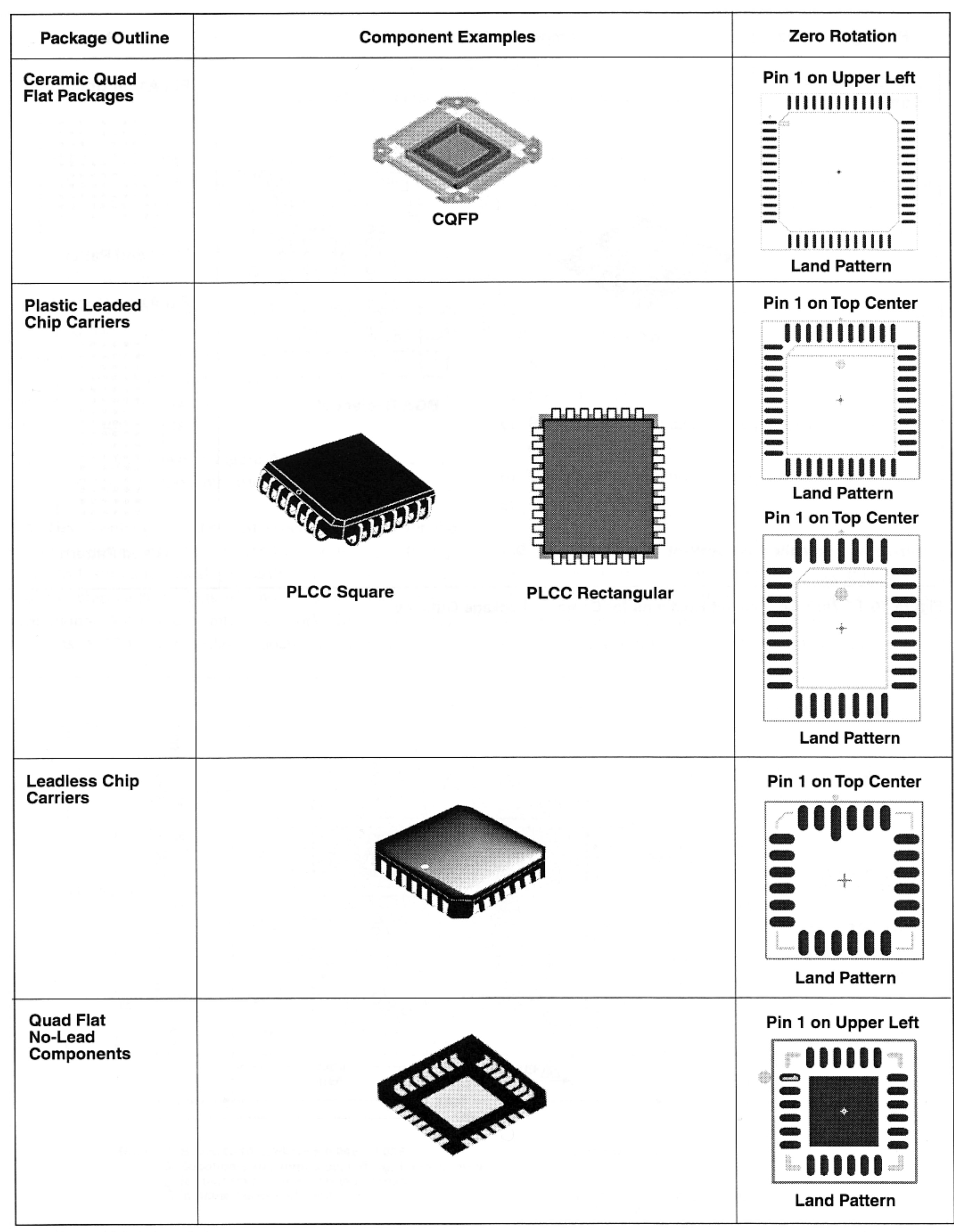



**Figure 16-1 Zero Component Rotations for Common Package Outlines (continued)**

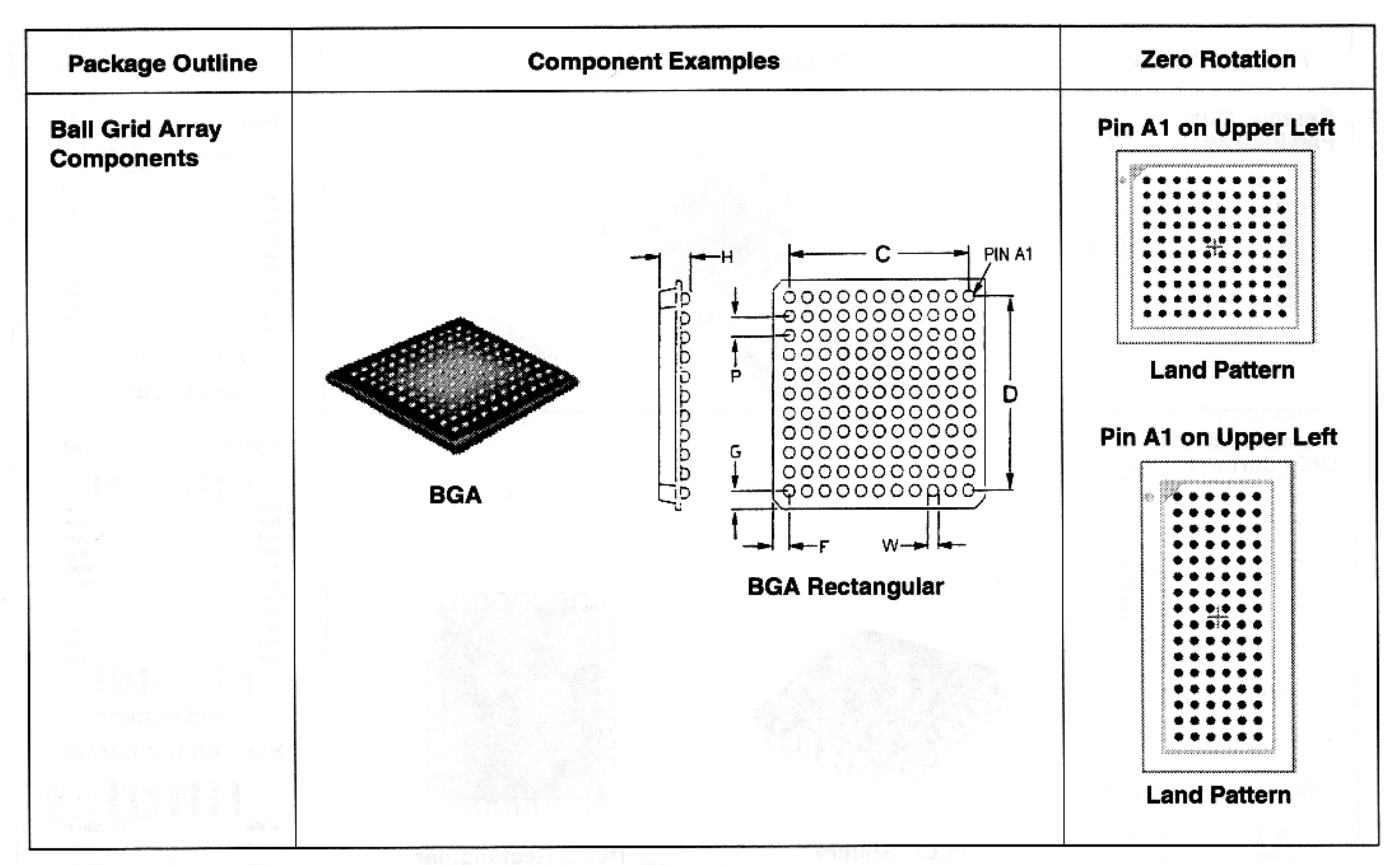



**Figure 16-1 Zero Component Rotations for Common Package Outlines**

# Appendix A
# (Informative)
# Test Patterns – Process Evaluations

The following test patterns have been developed as standards that may be used for the evaluation of standard board materials, with a variety of standard parts. IPC-A-49 artwork is available for these tests. The land patterns represent land pattern designs from the original IPC-SM-782 land pattern standard.

The test specimen contains conductors and plated-through holes and parts connected in a single daisy chain. One end of the daisy chain is connected to a common ground while the other end of the chain is connected to land patterns, then to a plated-through hole in which a wire may be soldered for test purposes.

Circuits that are shown in Figure A-1 and Figure A-2 contain the various components listed:

**A.1 Test Vehicle** Another test specimen is used for the testing of printed board structures that are intended to provide P&I structures used primarily for the mounting of leadless chip carriers. This test board is described in surface mount Air Force Mantech artwork (IPC-A-48). The board is a 12-layer multilayer board which contains 38 positions for mounting leadless chip carriers used by a surface mount evaluation program to evaluate printed board and substrate materials. The test boards produced from this artwork may contain metal cores, or other planes that control the coefficient of thermal expansion of the P&I structure.

The following are some examples of the type of materials that may be used as the constraining core.

a) Nonorganic materials (alumina)
b) Porcelainized clad invar materials
c) Printed boards bonded to low-expansion support (metal or nonmetal)
d) Compliant layer constructions
e) Metal core boards

**A.2 Test Patterns - In-Process Validator** Test patterns to validate in-process conditions are encouraged to be incorporated into the panel of a printed board assembly. These designed-in land patterns provide special features for automatic optical inspection and visual inspection.

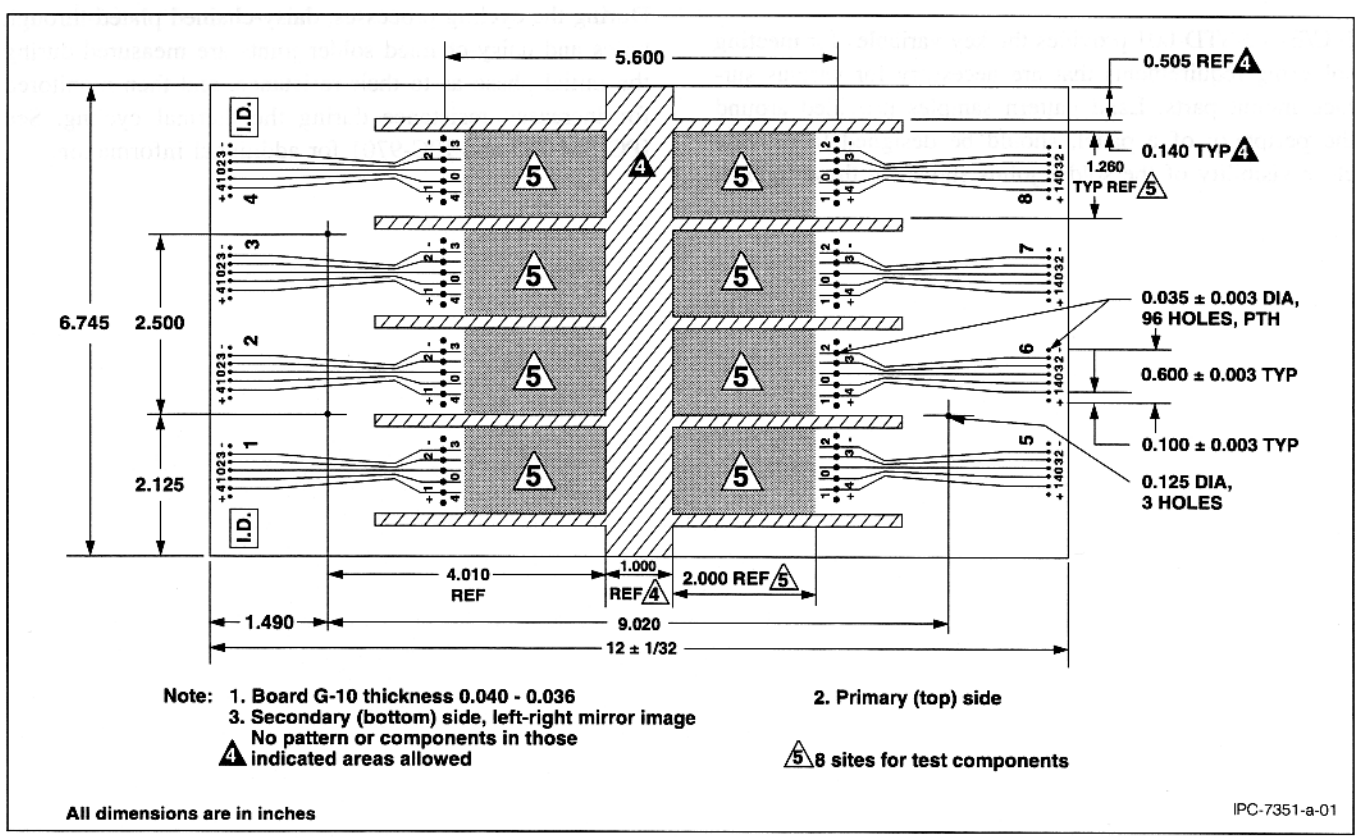



**Figure A-1 General Description of Process Validation Contact Pattern and Interconnect**

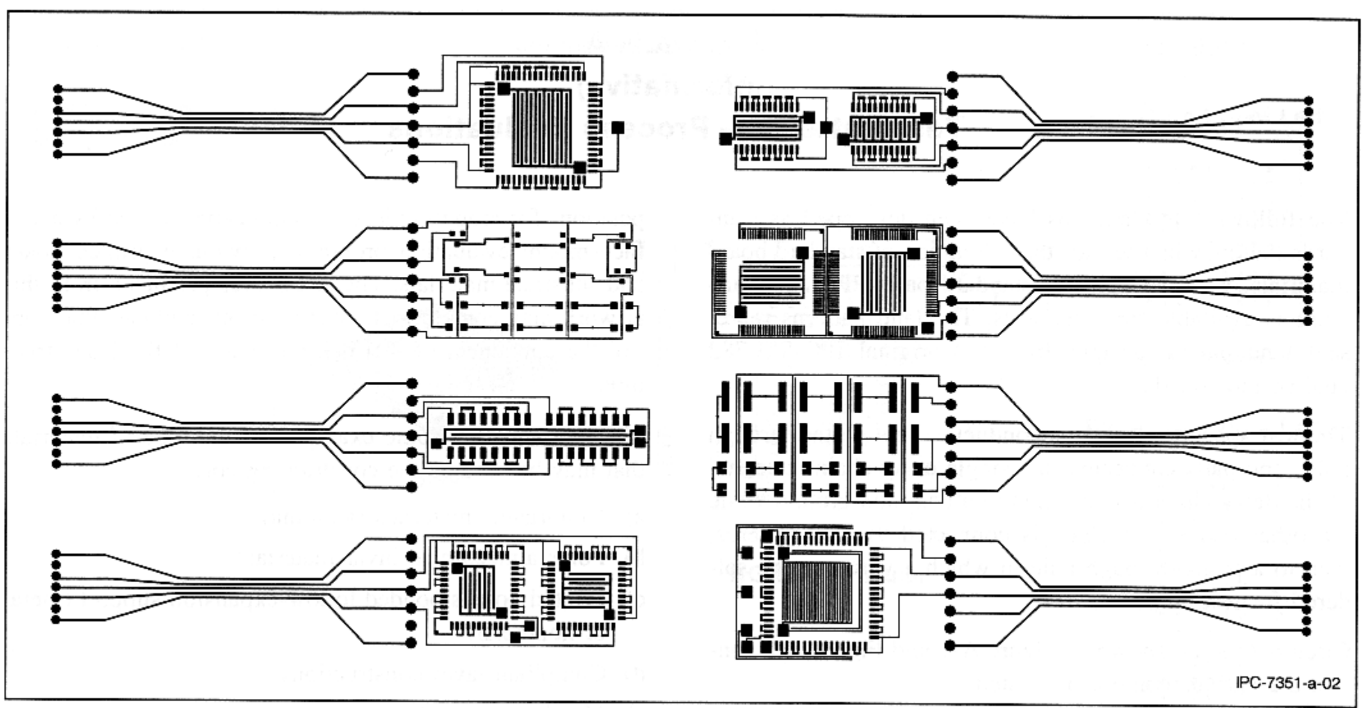



**Figure A-2 Photoimage of IPC-A-49 Test Board for Primary Side**

The land patterns are shown in documentation designed to provide a clear view of the soldering characteristic in such a way that land geometry is visible, and solder joint evaluation can be achieved. The same in-process validator is used to check the registration of solder paste prior to reflow soldering.

IPC/EIA J-STD-001 provides the key variables for meeting soldering requirements that are necessary for various surface mount parts. Land pattern samples provided around the periphery of a panel, should be designed to provide clear visibility of the solder joints shown in these figures.

**A.3 Stress Testing** Stress testing usually consists of temperature cycling of the printed board assembly that has been surface mounted through various extremes. The temperature cycling of the assembly or a coupon may be variety of cycling exposure (see Table 3-16).

During the cycling processes, daisy-chained plated-through holes and daisy-chained solder joints are measured during the initial phase as to their resistance, and then monitored for increased resistance during the thermal cycling. See IPC-SM-785 and IPC-9701 for additional information.

# Appendix B
# (Informative)
# Abbreviations and Definitions

| | |
|---|---|
| ATE | Automated Test Equipment |
| COB | Chip-on-Board |
| CTE | Coefficient of Thermal Expansion |
| DIP | Dual-in-Line Package |
| DTP | Diameter of True Position |
| FTP | Fine Pitch Technology |
| IC | Integrated Circuit |
| ICT | In-Circuit Test |
| IR | Infrared |
| LMC | Least Material Condition |
| MMC | Maximum Material Condition |
| OA | Organic Acid |
| OSP | Organic Solderability Protection |
| PB | Printed Board |
| PTFE | Polytetrafluoroethylene |
| PTH | Plated-through Hole |
| RA | Rosin Activated |
| RFS | Regardless of Feature Size |
| RMA | Resin Mildly Activated |
| RMS | Root Mean Square |
| SA | Synthetic-Activated |
| SFA | Standard Fabric Allowances |
| SIP | Single In-Line Package |
| SMA | Synthetic Mildly Activated |
| SMOBC | Solder Mask Over Bare Copper |
| SMT | Surface Mount Technology |
| SOIC | Small Outline Integrated Circuit |
| THT | Through-Hole Technology |

# APPENDIX C
# IPC-7351 Land Pattern Viewer

The IPC-7351 Land Pattern Viewer, hereafter referred to as the IPC-7351 LP Viewer, is a shareware program that allows users to view component and land pattern dimensional data in tabular form as well as graphical images that illustrate how a component is attached to the land pattern on the board. The IPC-7351 LP Viewer is provided on a CD-ROM that is included with the IPC-7351 standard. Updated versions of the program, including dimensional data for new component families, can be downloaded for free from **www.ipc.org** under the "PCB Tools and Calculators" link.

**C.1 Software Installation** The IPC-7351 LP Viewer comes on CD-ROM in a zipped file format. The zip file contains important text files on the usage of the shareware program as well as installation requirements. Microsoft .NET Framework is required for the IPC-7351 LP Viewer to run properly. If you have determined that you do not have this component, the installation requirement text file details how to obtain this software. Once you have confirmed that your system has Microsoft .NET Framework, you can select the executable IPC-7351 LP Viewer file to begin the installation process. See the Users Guide within the IPC-7351 LP Viewer for detailed instructions on the download of .NET Framework.

**Note:** A special file is required for the eventual build of user preferences; this file has the extension [.dat]. The IPC-7351 LP Viewer program installation does not initially include a [.dat] file and therefore one is created automatically the first time you run the program. When starting the program for the first time, the User will be prompted by a message that states a .DAT file does not exist and that one is being created. A second message will be displayed confirming that the file has been created.

**C.2 Software Usage** Once installed, select the "Users Guide" tool bar button located on the main interface screen for the IPC-7351 LP Viewer. This .pdf document helps in familiarizing the user with the Viewer by providing detailed information on the following:

- Software Installation
- Setting up User Preferences
- Operating the Search Library Menu
- Updating Parts Library Files

**C.3 Software Updates** The IPC-7351 LP Viewer relies on library files for component and land pattern dimensional data. The extension for the library files is [.p]. These .p files provide the raw dimensional data necessary for the software to display components and land patterns in graphical forum.

.p files also contain parts attributes. Attributes hold vital statistical and descriptive data that every land pattern needs so other users can quickly identify the component characteristics. Attributes help organize data used to search for existing library parts. Detailed descriptions of how to utilize attributes can be found by selecting the "Users Guide" tool bar button located on the main interface screen for the IPC-7351 LP Viewer.

As new component families are standardized by the industry, new .p library files will be made available to users of the IPC-7351 LP Viewer. These updated .p files can be downloaded for free from **www.ipc.org** under the "PCB Tools and Calculators" link.

**C.4 Software Upgrades** The IPC-7351 LP Viewer is a shareware program that allows users to search and display existing land patterns for standardized component families. The Viewer is supported by additional software tools that allow for the calculation of new land patterns as well as the creation of new part libraries that stores new component and land pattern data. Information on these enhanced software tools is available at **www.ipc.org** under the "PCB Tools and Calculators" link.

## Technical Questions

The IPC staff will research your technical question and attempt to find an appropriate specification interpretation or technical response. Please send your technical query to the technical department via:

tel: 847-615-7100
fax: 847-615-7105
www.ipc.org
e-mail: answers@ipc.org

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IPC technical forums are opportunities to network on the Internet. It's the best way to get the help you need today! Over 2,500 people are already taking advantage of the excellent peer networking available through e-mail forums provided by IPC. Members use them to get timely, relevant answers to their technical questions. Contact KeachSasamori@ipc.org for details. Here are a few of the forums offered.

### TechNet@ipc.org

TechNet forum is for discussion of issues related to printed circuit board design, assembly, manufacturing, comments or questions on IPC specifications, or other technical inquiries. IPC also uses TechNet to announce meetings, important technical issues, surveys, etc.

### ComplianceNet@ipc.org

ComplianceNet forum covers environmental, safety and related regulations or issues.

### DesignersCouncil@ipc.org

Designers Council forum covers information on upcoming IPC Designers Council activities as well as information, comments, and feedback on current designer issues, local chapter meetings, new chapters forming, job opportunities and certification. In addition, IPC can set up a mailing list for your individual Chapter so that your chapter can share information about upcoming meetings, events and issues related specifically to your chapter.

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### leadfree.ipc.org

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Subject:
Message: subscribe TechNet Joseph H. Smith

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Subject:
Message: signoff DesignerCouncil

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IPC-7351

# Generic Requirements for Surface Mount Design and Land Pattern Standard

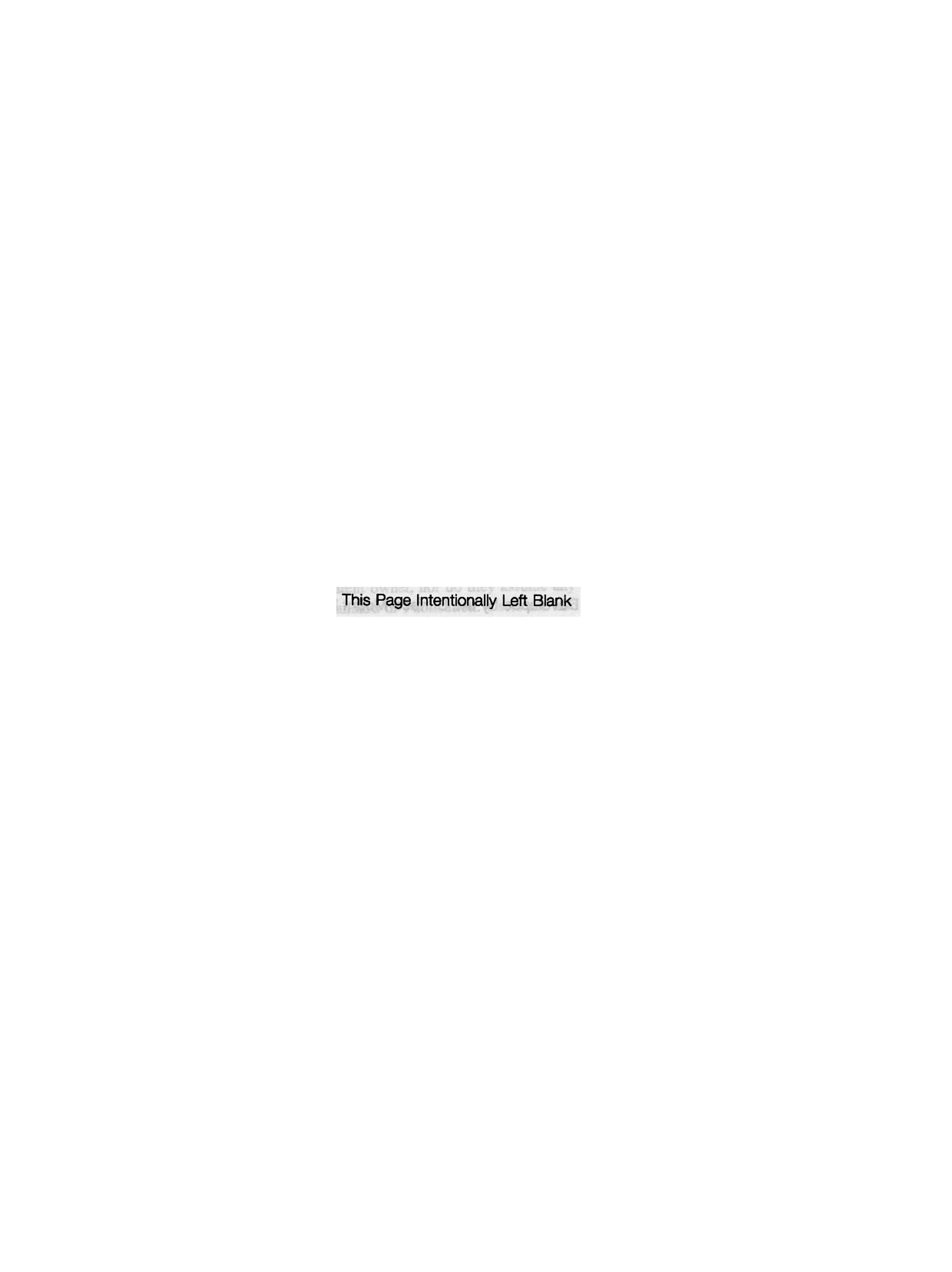
Developed by the Surface Mount Land Patterns Subcommittee (1-13) of the Printed Board Design Committee (1-10) of IPC

***Supersedes:***
IPC-SM-782A with
Amendments 1 & 2

Users of this publication are encouraged to participate in the development of future revisions.

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# Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the Surface Mount Land Patterns Subcommittee (1-13) of the Printed Board Design Committee (1-10) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

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